

IBTA 32 Port VNA MOI for FDR and EDR Cable Tests

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Table 1: Modification Record

Revision	Release Date	Author	Comments
1.00	10/24/2016	Mike Bogochow	<ul style="list-style-type: none">• Updated for 32 port PNA.
1.01	12/9/2016	Rupert Dance	<ul style="list-style-type: none">• Updated spec versions, Agilent to Keysight Acknowledgements• Updated all the S-Parameter Specs to match Spec version 1.4• Updated Procedure for Active Cables for the s32p process
1.02	4/11/2017	Mike Bogochow	<ul style="list-style-type: none">• Updated spec version and fixed S parameter equations
1.03	4/12/2018	Rupert Dance OJ Danzy	<ul style="list-style-type: none">• Added QSFP-DD Procedure

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ELECTRICAL SIGNALING CHARACTERISTICS

Overview:

This test procedure was written to explain how to use the Keysight PNA Network Analyzer (32 port models) to make the measurements required per the InfiniBand Architecture Specification Volume 2 Release 1.4 FDR, EDR and HDR cables and connectors.

References

InfiniBand Architecture Specification Volume 2 Version 1_4.2016-11-16

General Resources Requirements

See [Appendix A](#) for IBTA Specifications.
See [Appendix B](#) for FDR measurement specifications.
See [Appendix C](#) for EDR measurement specifications.

Initial Setup for Keysight PNA

This section contains notes regarding the setup for testing InfiniBand FDR and EDR cables using the Keysight PNA Network Analyzer, specifically the Keysight N9375A network analyzer (see Figure 1).

Passive Cables - A “Passive” cable is one that is either: Unequalized, equalized in connector, or equalized in wire.

Limiting Active Cables – A “Limiting Active” cable is one that has active electrical components that act as nonlinear limiting devices in both connectors and may utilize either a copper interconnect or an optical fiber. A special case of a "Half Active" cable is one that utilizes a Copper interconnect and has active electrical components that act as nonlinear limiting devices in only one of the connectors.

The CIWG test procedures test the worst case lane of the cables submitted for testing. The worst case lane is determined by using the Mellanox Eye Opening test procedure which is described in a separate Method of Implementation (MOI) which is available on the IBTA website.

The following procedures are valid for both passive and active FDR and EDR cable testing except that Insertion Loss, NEXT, and FEXT measurements are not performed on Active Limiting cables.

Perform an instrument warm-up and compensation according to the user manual of the network analyzer before connecting the 3.5mm cables and Module Compliance Boards (MCB).

Initial Setup Procedure

- 1) Compensate for any temperature changes by connecting 50 ohm terminators on all ports and running the temperature compensation algorithm on the PNA.
- 2) Connect 3.5 mm cables to PNA. Refer to Figure 27 for the physical port assignment of the PNA.
- 3) Perform calibration if not already done. Refer to Appendix D – PNA Calibration.
- 4) Connect 3.5 mm cables to MCBs. Refer to Physical Configuration in Appendix E – DUT Configuration.

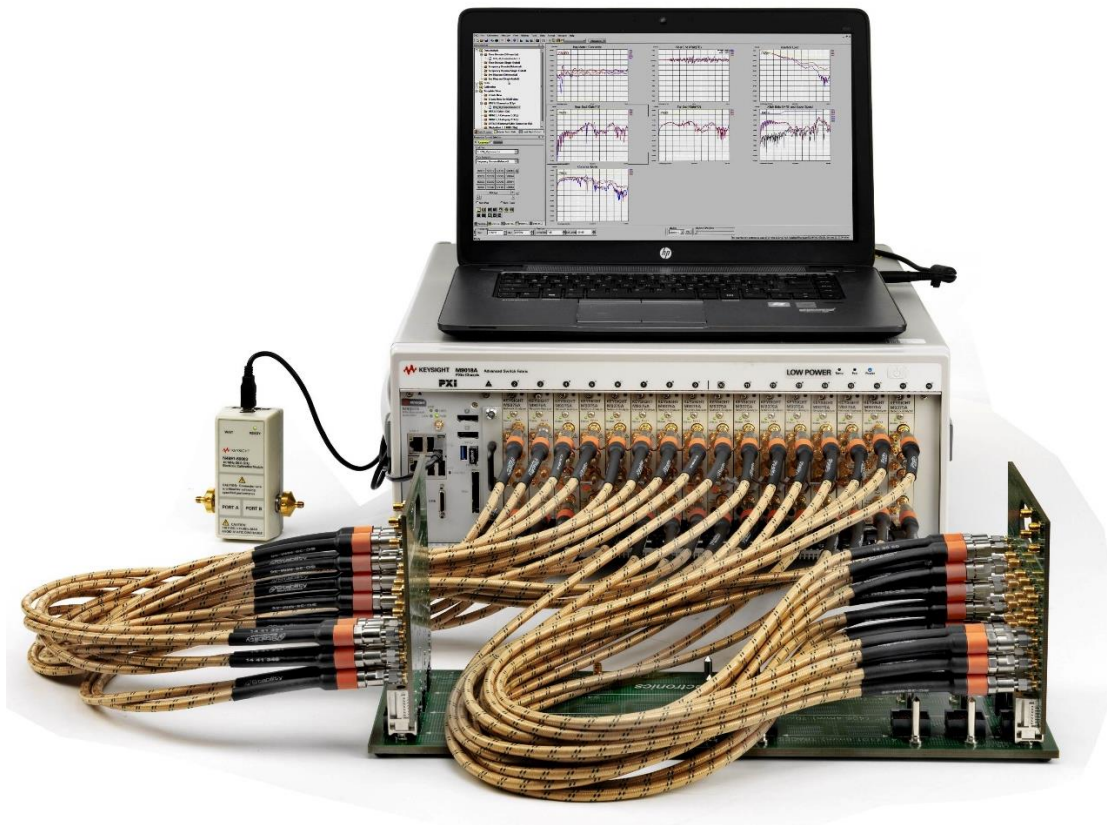


Figure 1 – Keysight N9375A PNA

Procedure for Passive Cables

High Level Description

- 1) Start new measurement in Keysight Physical Layer Test System (PLTS) software.
- 2) Run the measurement.
- 3) Post process the s32p files using PLTS.
- 4) Post process the s32p files using Matlab scripts.

Detailed Description

- 1) In the PLTS software, click File → New

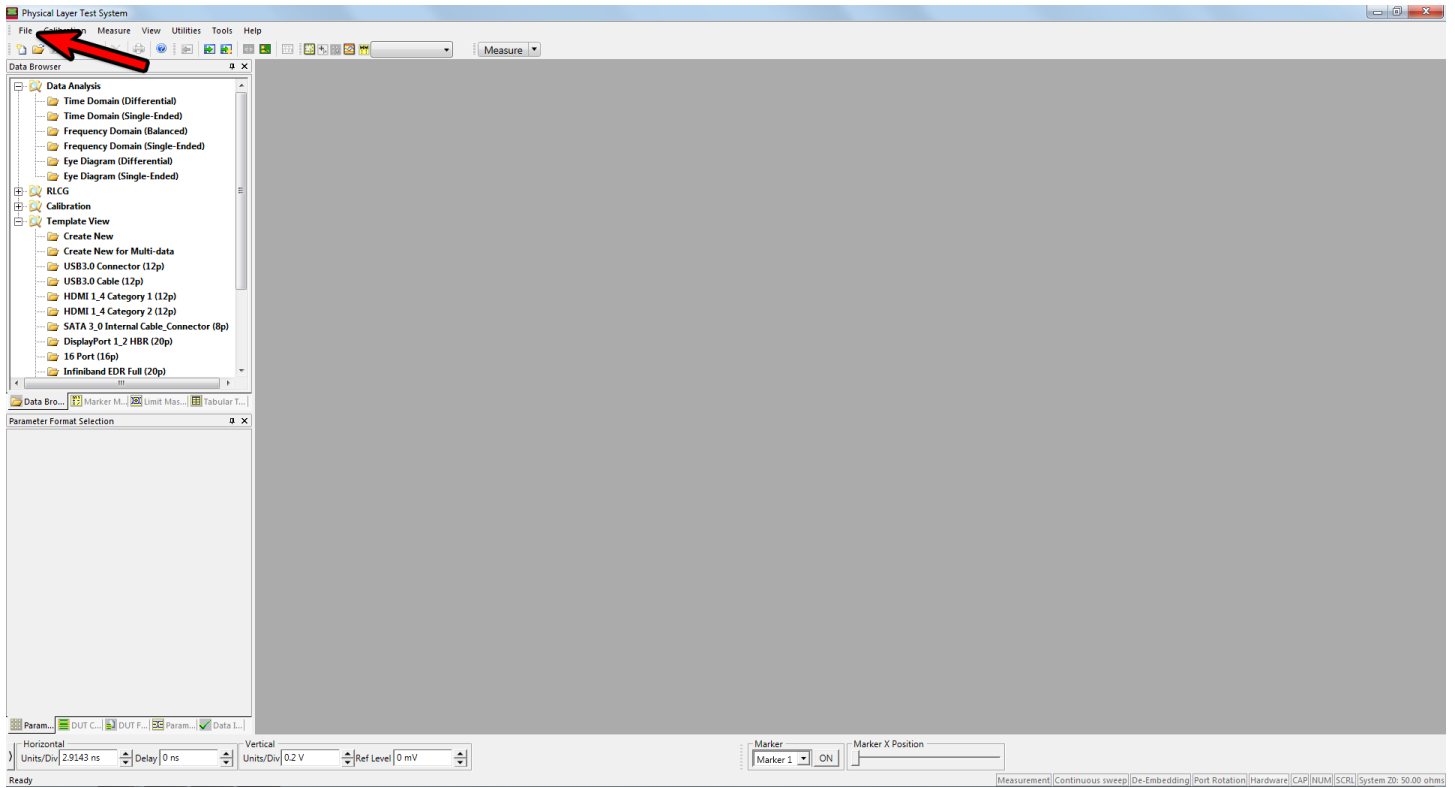


Figure 2 – PLTS new measurement

2) Select New Measurement, then click Next

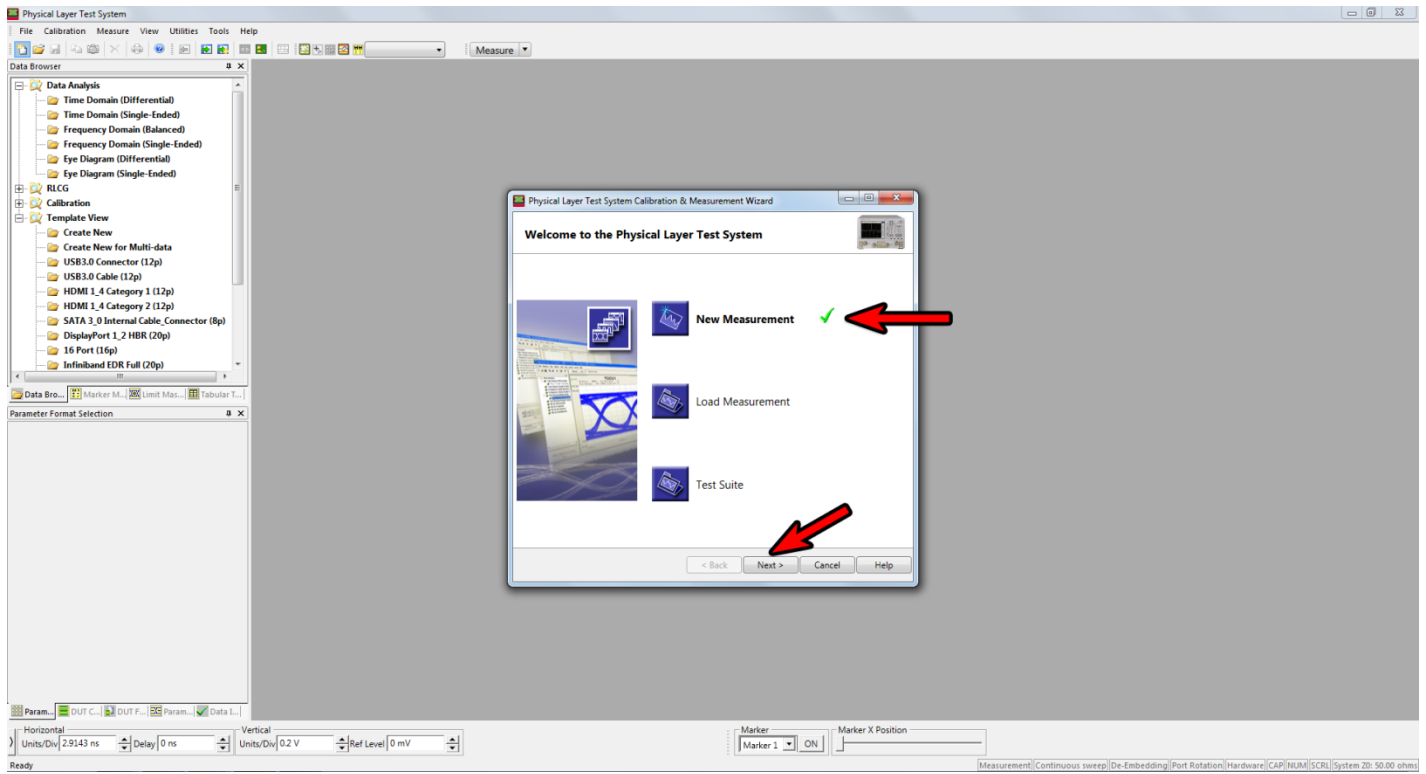


Figure 3 - PLTS measurement wizard

3) Click Edit under the DUT Configuration section

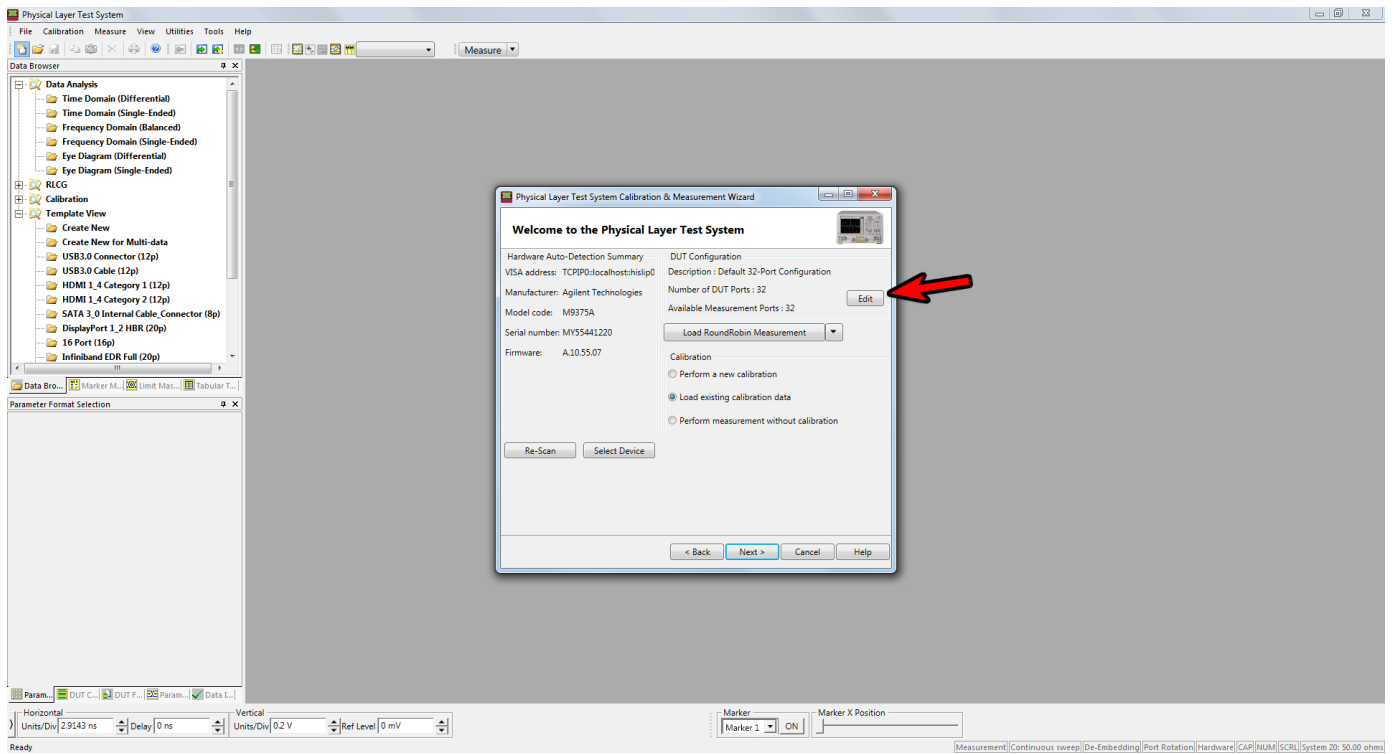


Figure 4 - PLTS select DUT configuration

- 4) Load an existing DUT configuration file by pressing the Load button and click OK. If a DUT configuration has not already been set up, refer to Appendix E – DUT Configuration.

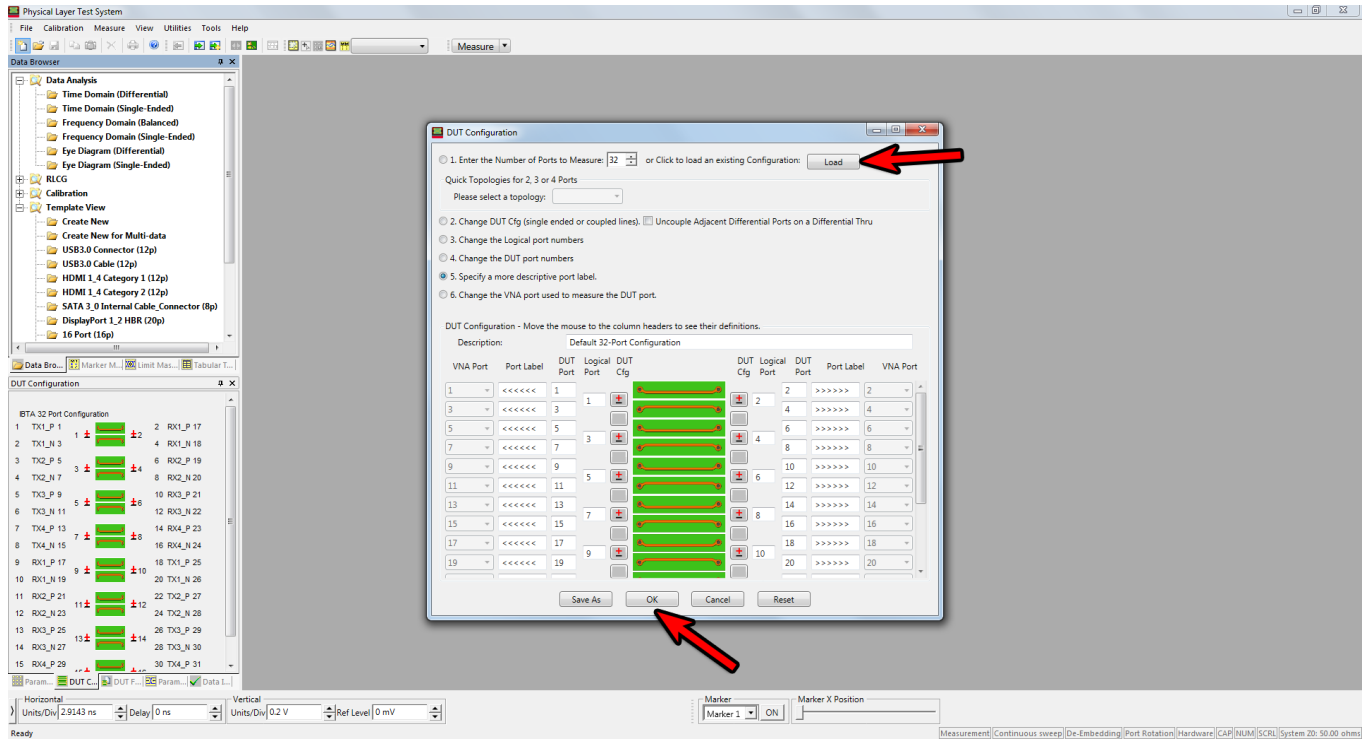


Figure 5 - PLTS Load DUT configuration

- 5) Select Load existing calibration data under the Calibration section, then click Next. If calibration has not already been performed, refer to Appendix D – PNA Calibration.

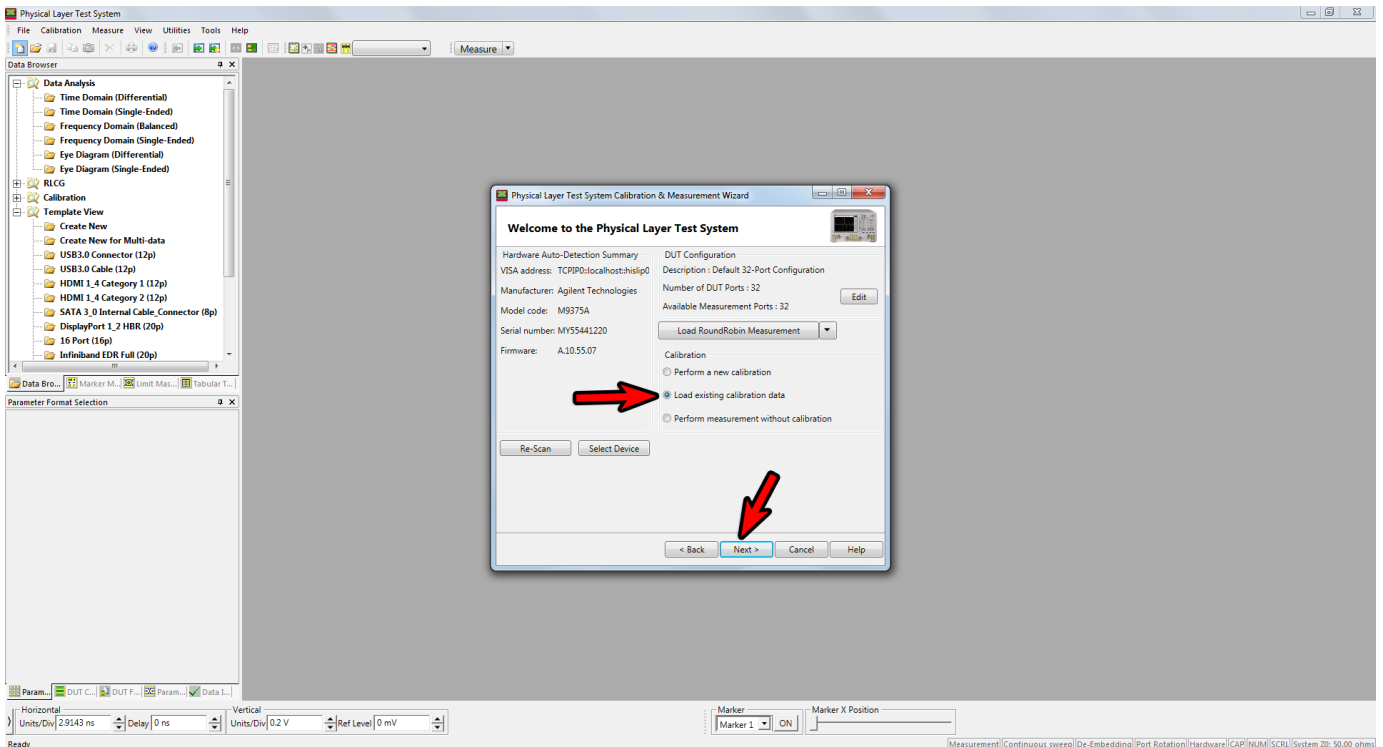


Figure 6 - PLTS load existing calibration data

6) Select the calibration to load, then click Next

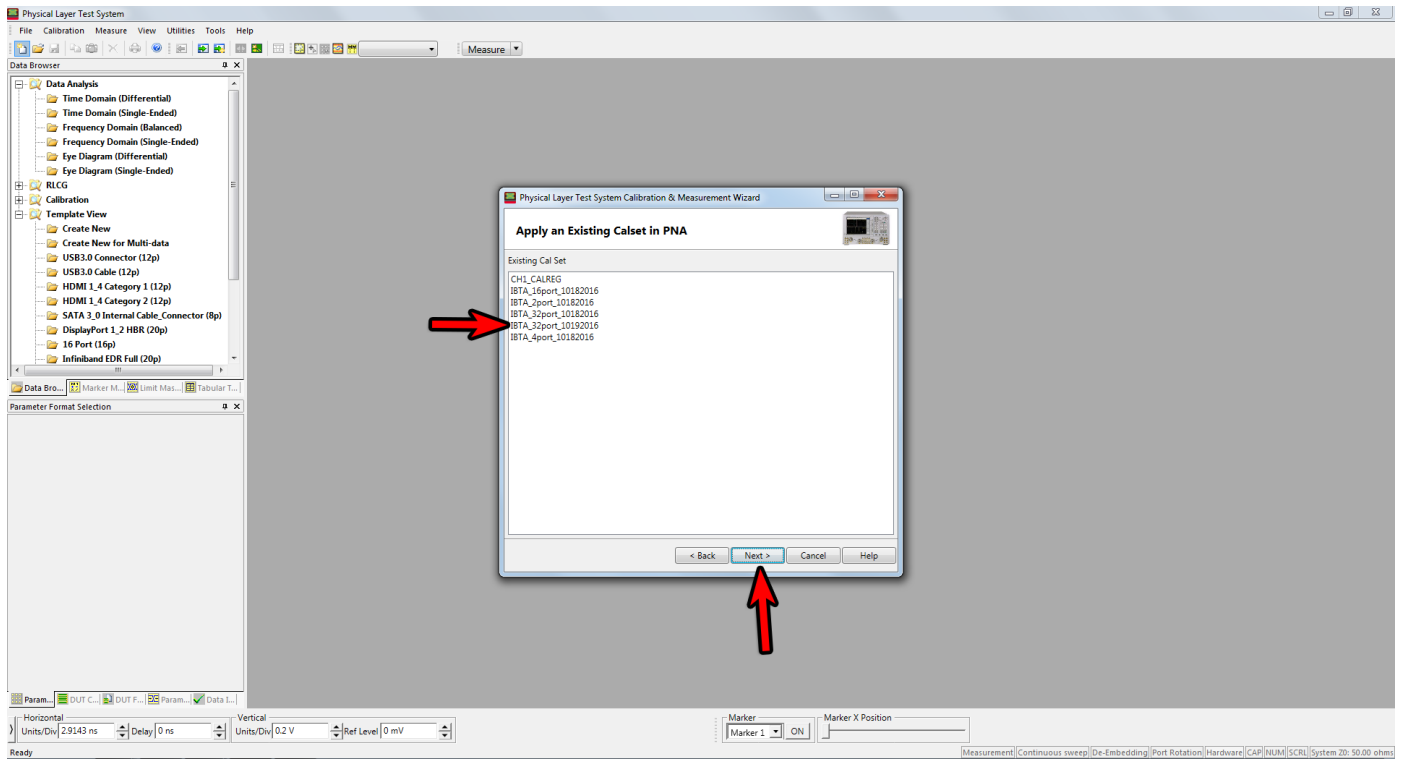


Figure 7 – PLTS apply existing calset in PNA

7) Click Next.

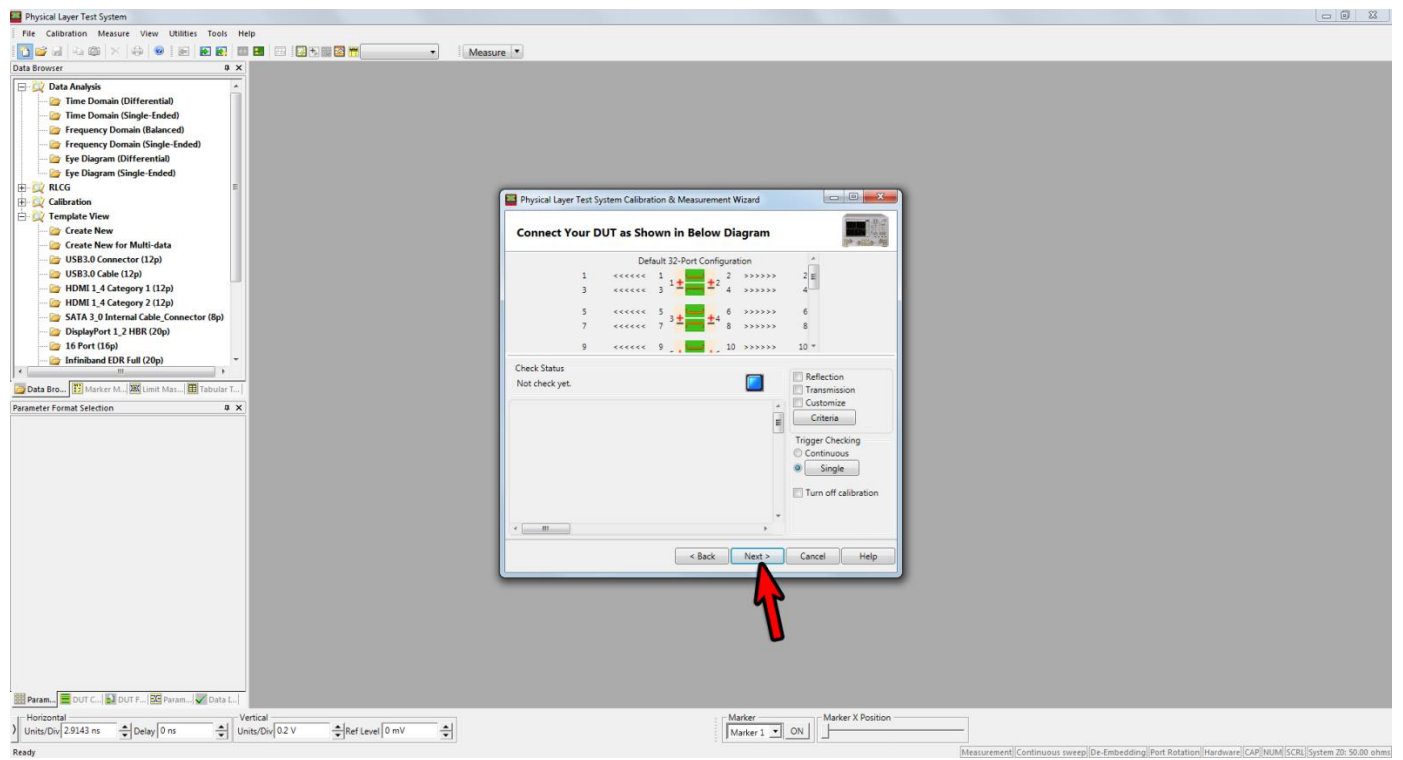


Figure 8 - PLTS DUT status check

- 8) Check the Change Measurement Settings checkbox.
- 9) Enter 10 kHz in the IF Bandwidth text field.
- 10) Click Measure.

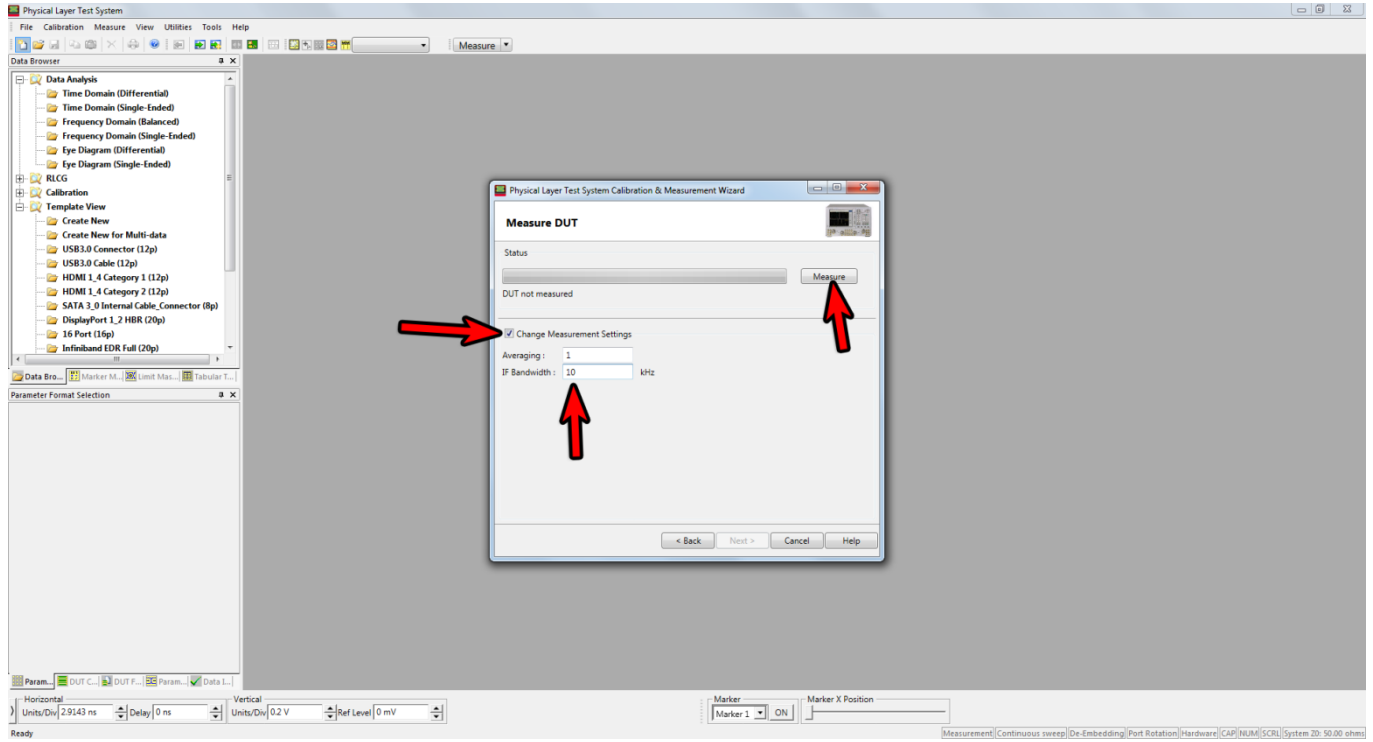


Figure 9 - PLTS change measurement settings and perform measurement

- 11) Once measurement is complete, click Next.

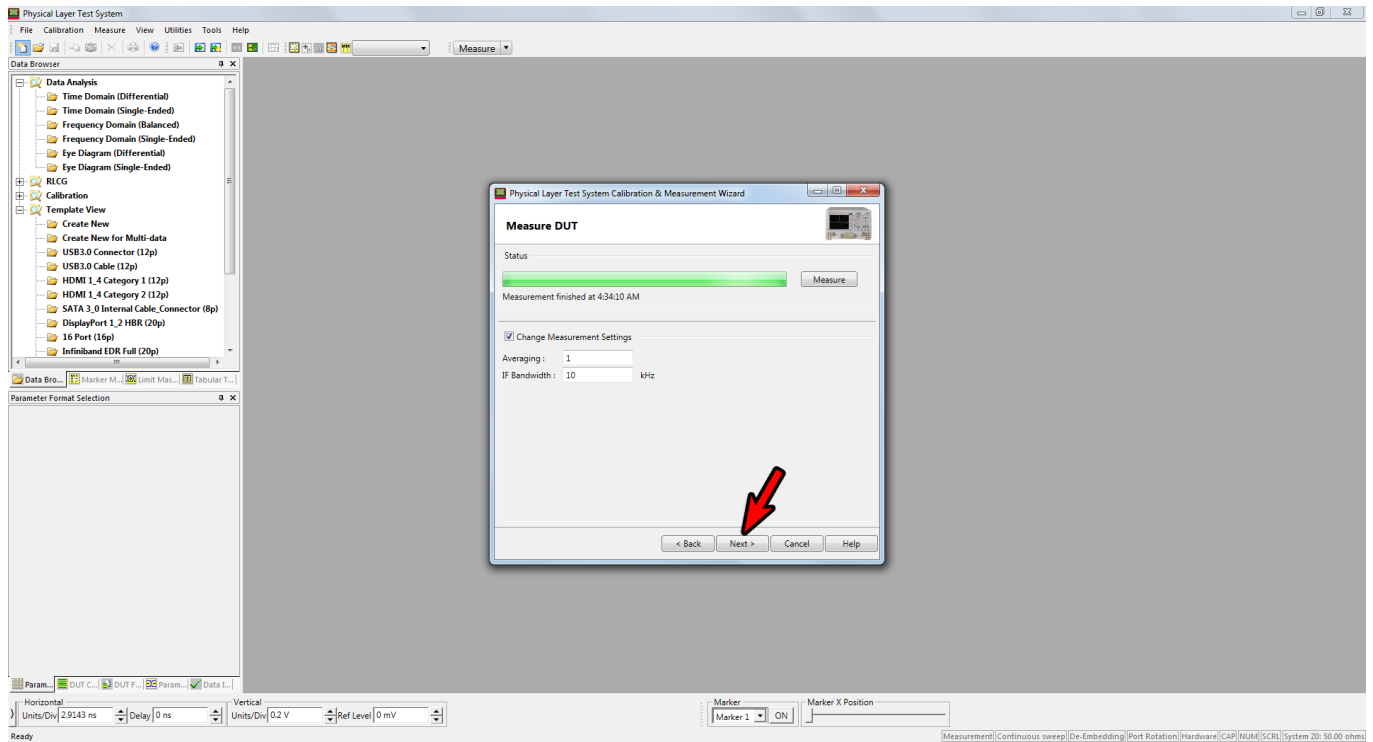


Figure 10 - PLTS finish measurement

12) Select the desired analysis view template, then click Next.

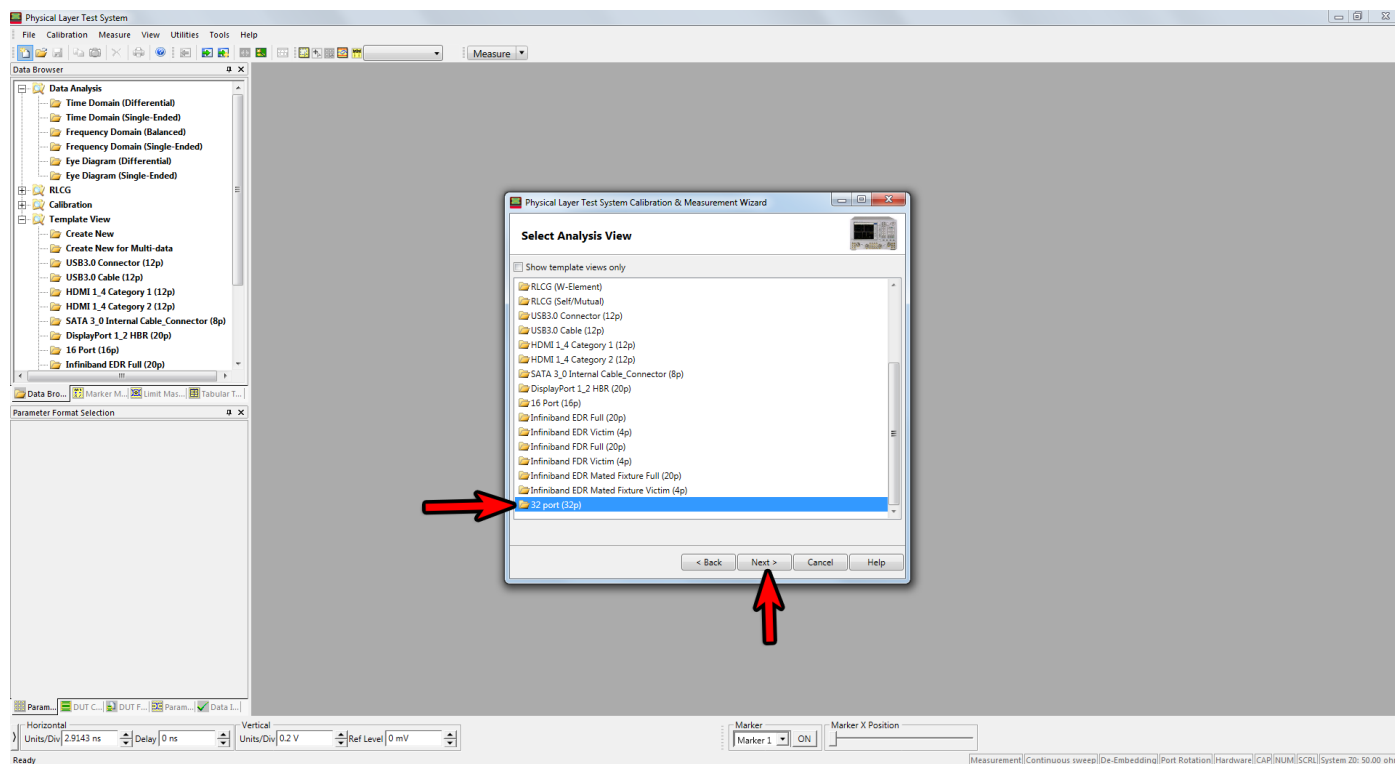


Figure 11 - PLTS select analysis view template

13) Click Next.

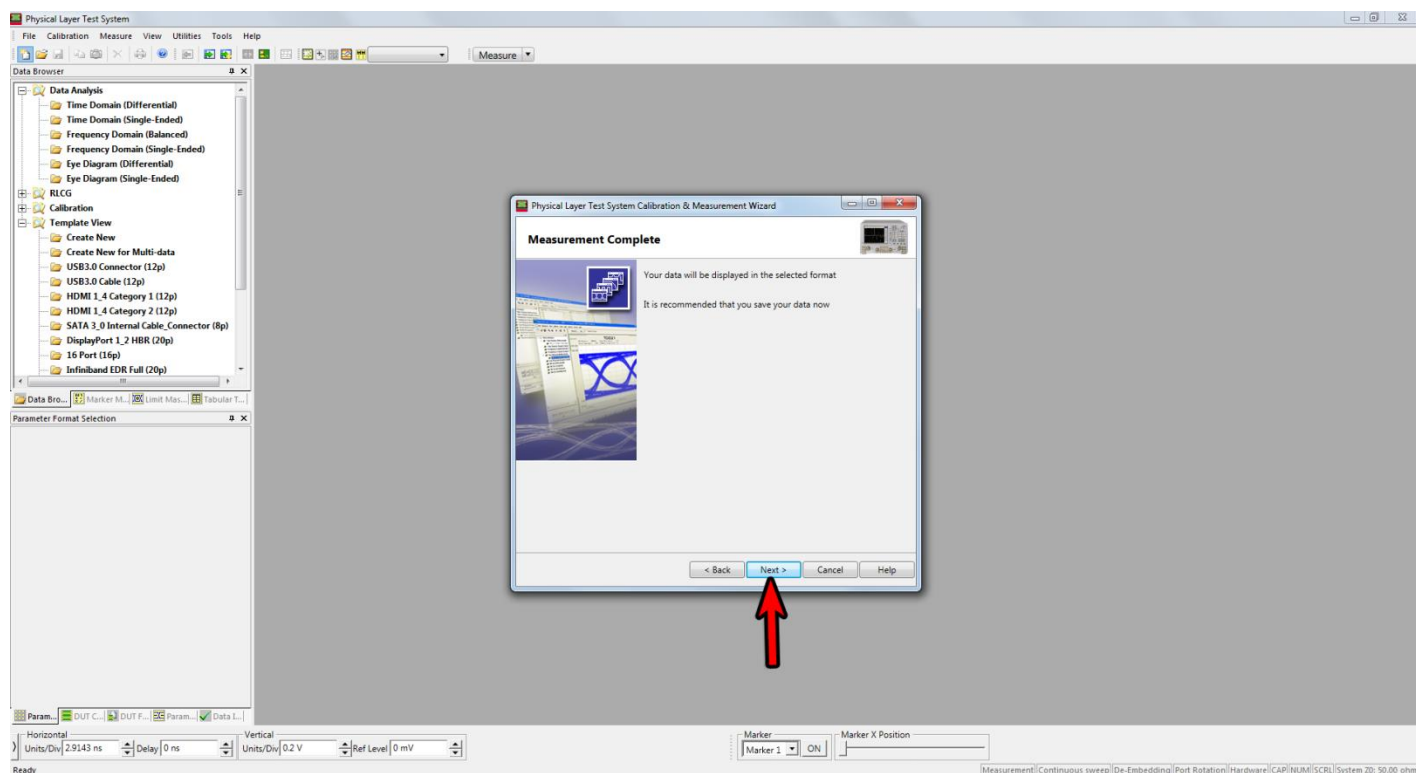
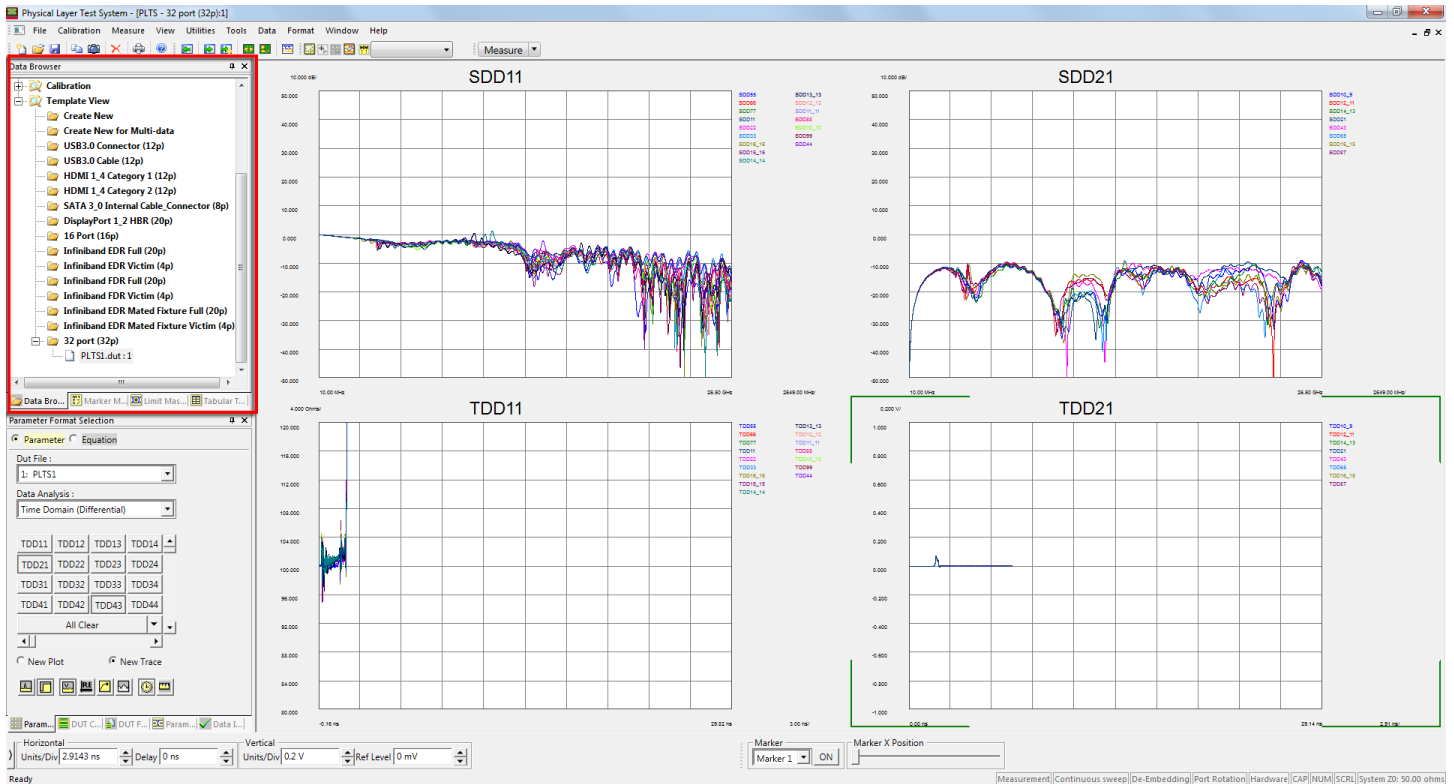


Figure 12 - PLTS finish measurement wizard

14) The selected analysis view will now be displayed. You can select another template from the menu on the left to load with the same data.



15) Save the PLTS results:

- a) Press Export button on toolbar to save .s32p file. This button is shown in the right red box in Figure 13.
 - i) Click Browse to specify the file to save to
- b) Press Export Bitmap button on toolbar to save screenshot of the graphs. This button is shown in the left red box in Figure 13.
 - i) Select desired image resolution. It is recommended to select the highest available.
 - ii) Specify the file to save to. It is recommended to change the image format to png.

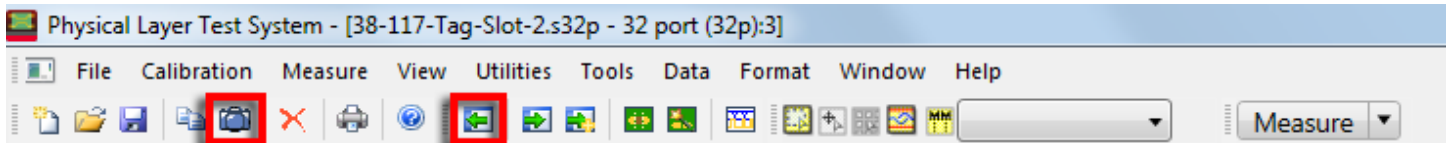


Figure 13 - PLTS toolbar export

16) Perform next measurement. You do not need to create a new measurement for the next cable. Just swap out the cable and click the measure button on the toolbar as shown in Figure 14.

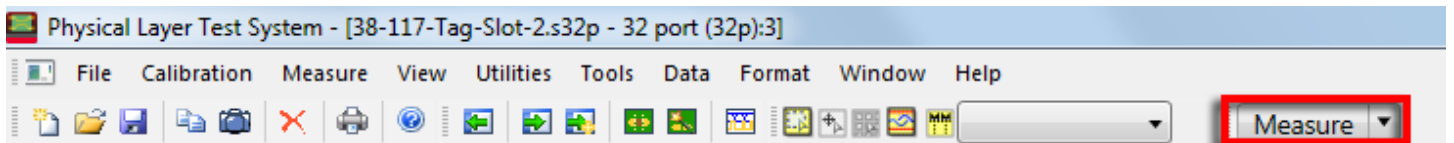


Figure 14 - PLTS toolbar measure

Procedure for Active Cables

The PLTS procedure for active cables is the same as for passive cables but there are different setup requirements:

- 1) Only connect the DUT to one MCB (MCB-B) at any time (however, both MCBs remain connected to the PNA)
- 2) Both MCBs must be powered
- 3) The other end of the cable should be connected to a switch which continuously transmits data
 - a) This is being provided by Mellanox engineers who configure one of their switches to continuously transmit a PRBS9 pattern from one of the ports which is connected to the opposite end of the AOC from the one connected to the MCB and the Keysight VNA.

The testing is performed twice, once for each direction. That is, one side of the cable is plugged into the MCB and the other is plugged into the switch for the first phase of testing and then the sides of the cable are swapped for the second phase of testing.

The reason for this setup is because, during previous IBTA Plugfest testing, it was found that some DUTs are sensitive to whether both boards are powered and others are sensitive to whether MCB-A or MCB-B is powered. Therefore, in the past this test was run in all three combinations and the best results were taken.

For PF29 and PF30 we reviewed the AOC results with OJ from Keysight and we have restricted the results to measurements taken on the receive side (SCCxx, SDCxx and SDDxx) because of the test methodology we had to implement with Active Cables. We analyze the receivers on one side of the cable while the other side is plugged into a Mellanox switch transmitting a PRBS9 pattern. Then we flip the cable and take another measurement – this way we are measuring all 8 Rx lanes of the cable.

The Matlab code used to process s32p results from PF29 and later has been verified by using the PF29 code to reprocess some s4p files from PF28 and comparing them to the results obtained in PF28 using the old 4 port VNA and the old UNH-IOL Matlab code. When we see AOC failures, we also doubled check the Matlab derived results by using the Keysight PLTS application.

Post Processing

PLTS and Matlab

Keysight Physical Layer Test System (PLTS) software in combination with internal Matlab collaboration can process the data files to determine pass/fail for:

- a) Insertion Loss (SDD21), Fitted Insertion Loss (FIL), Insertion Loss Deviation (ILD) and ILDrms.
- b) Return Loss measurements
 - i. SDD11, SDD22, SCC11, SCC22
- c) Common Mode to Differential Reflection
 - i. SDC11, SDC22
- d) Integrated Common Mode Conversion Noise (ICMCN)
 - i. SCD21

To perform the Matlab processing through PLTS, simply load the corresponding analysis view template for an s32p results file. At Plugfest 30, these templates were called “InfiniBand EDR Full (32p)” and “InfiniBand FDR Full (32p)”.

Importing s32p Files into PLTS

If you would like to open up an existing s32p file for processing within PLTS, you must use the import functionality.

- 1) In the PLTS software, click File → Import
- 2) Click Browse and select the s32p file you would like to import

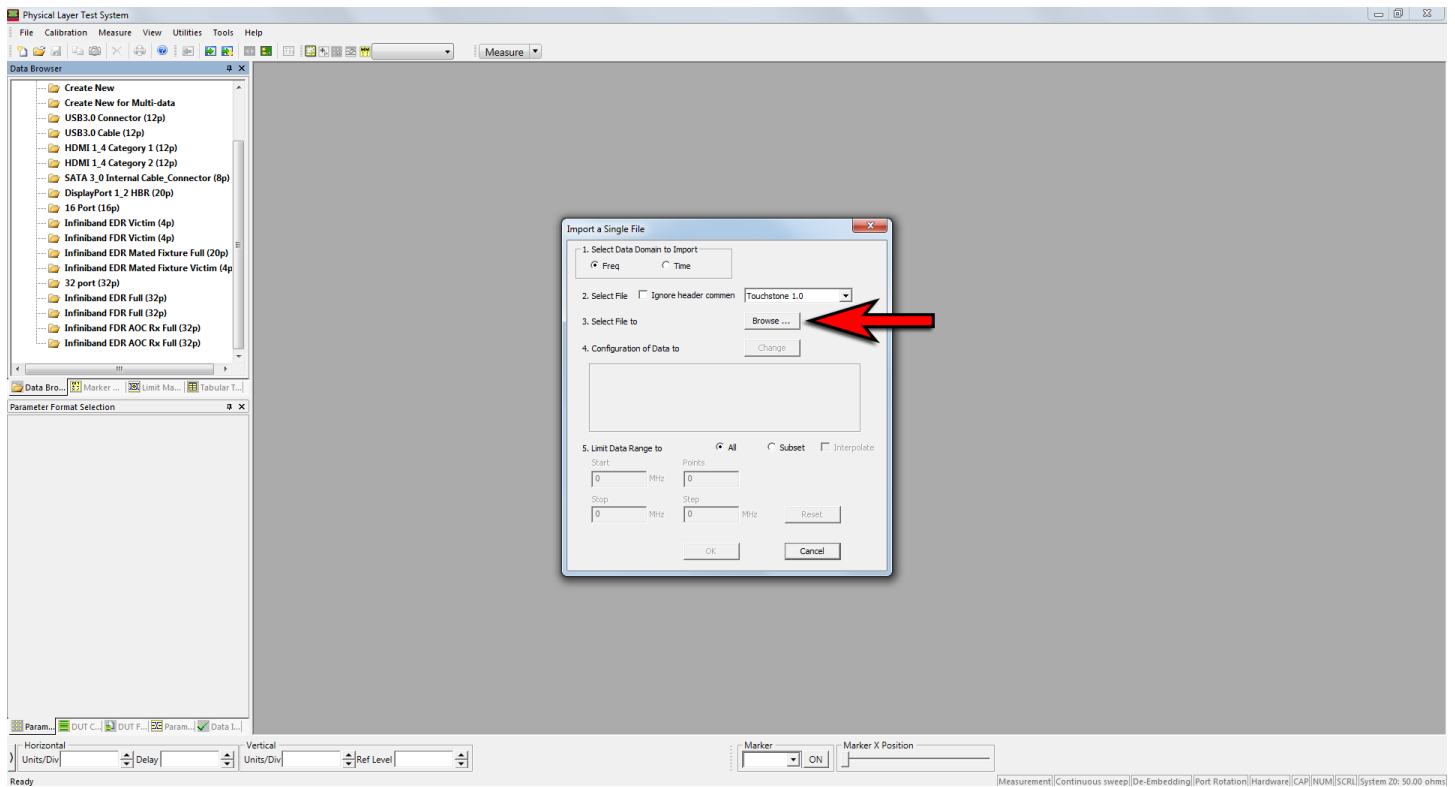


Figure 15 - PLTS import 23p file

3) Click OK

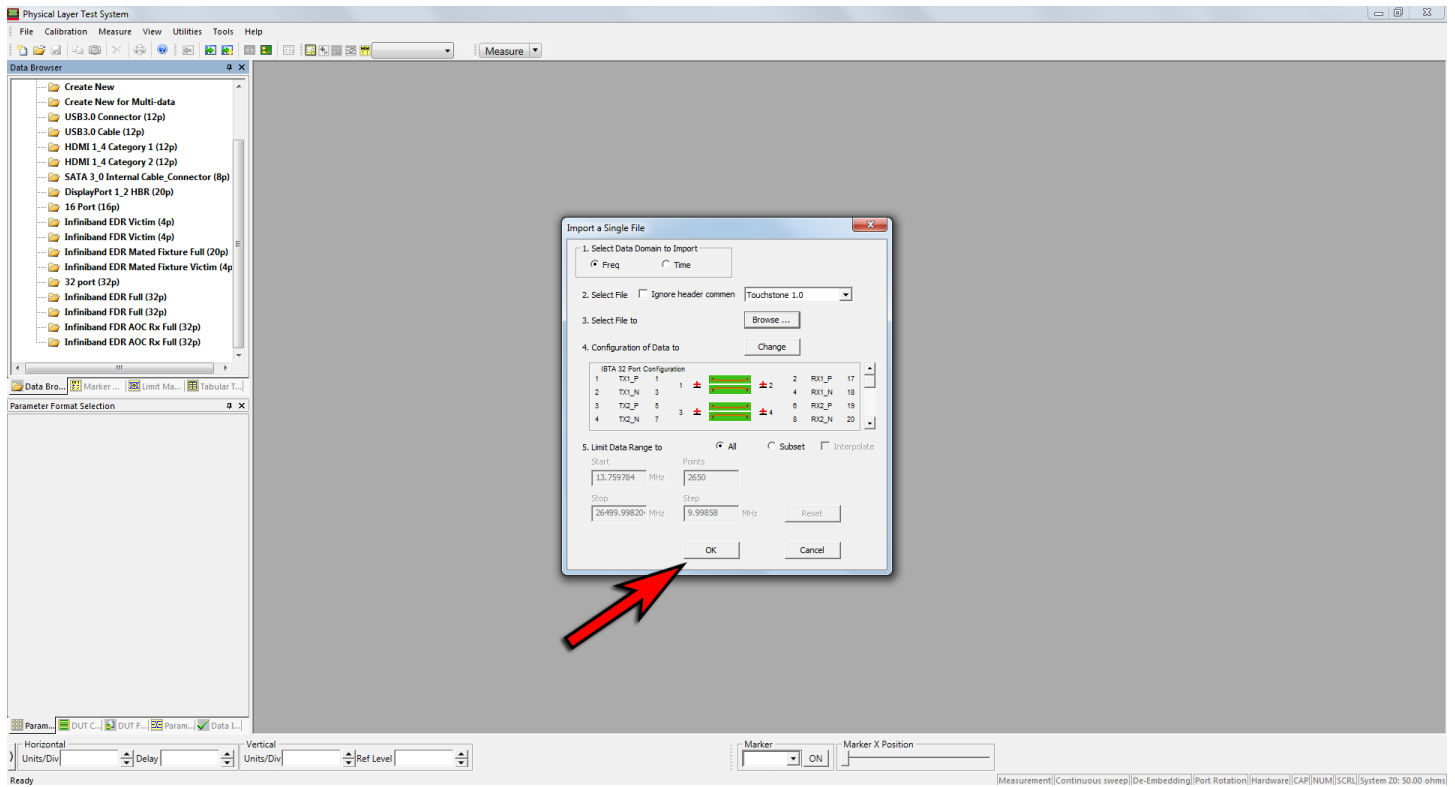


Figure 16 - PLTS finish import

4) Select the desired analysis view, then click OK

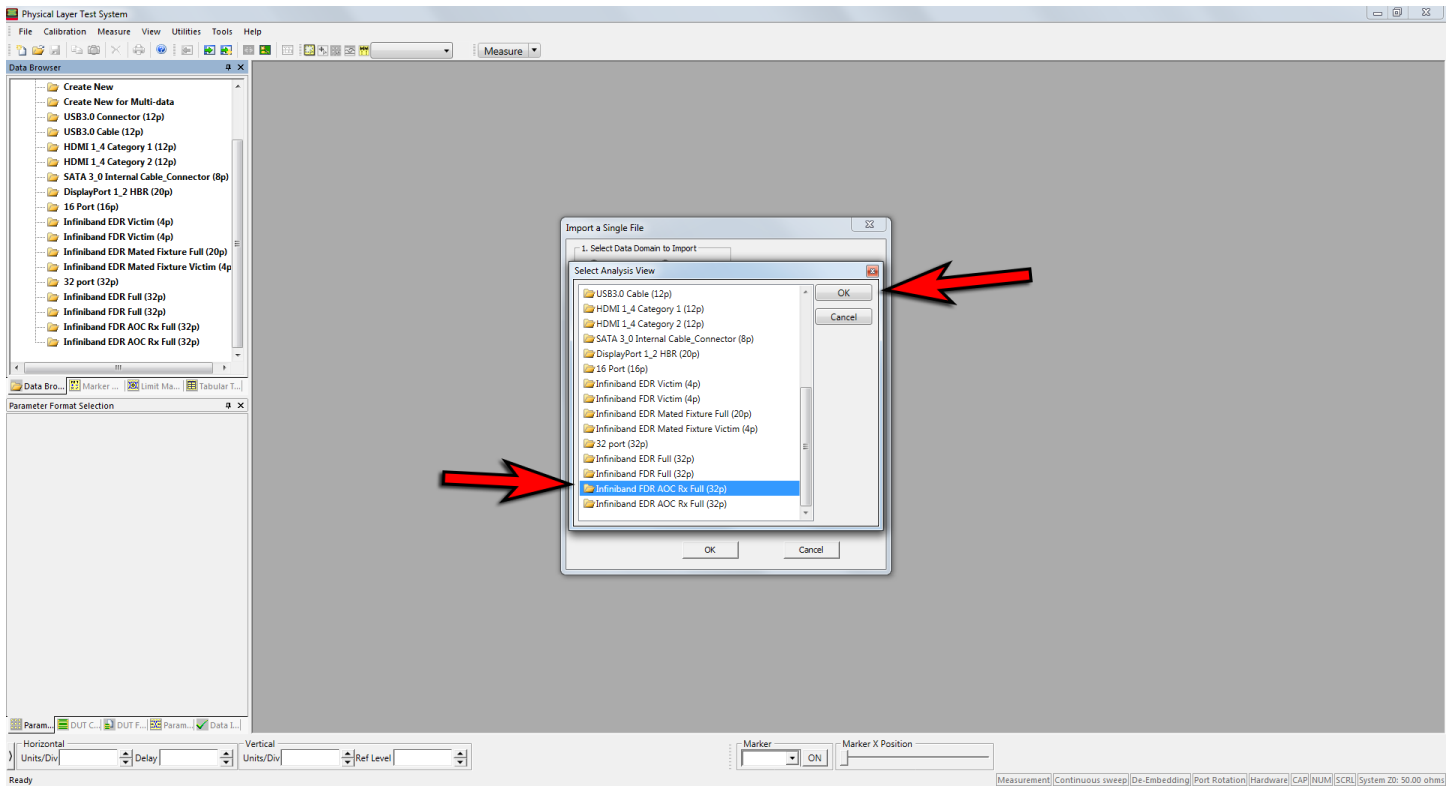


Figure 17 - PLTS set analysis view for imported file

Matlab post processing

TBD

Appendix A – Resource Requirements

- InfiniBand Architecture Specification Volume 2 Version 1.4.2017-04-06

Appendix B – FDR S Parameter Requirements

Table 2: FDR Insertion Loss

Description	Min Value	Max Value	Unit
Maximum insertion loss at 7.03125 GHz	-	15	dB
Maximum fitted insertion loss coefficient a_0	-0.75	0.5	dB
Maximum fitted insertion loss coefficient a_1	0	17.96	dB
Maximum fitted insertion loss coefficient a_2	0	10.25	dB
Maximum fitted insertion loss coefficient a_4	0	7.91	dB

Table 3: FDR Insertion Loss Deviation (ILD)

Frequency (GHz)	Min Value	Max Value	Unit
$0.05 \leq f < 3.50$	-0.75	0.75	dB
$3.50 \leq f < 7.00$	$0.75 - 0.4286 * f$	$0.4286 * f - 0.75$	dB
$7.00 \leq f \leq 10.5$	-2.25	2.25	dB

Table 4: FDR SDD11 and SDD22

Range (GHz)	Max Value (dB)
$0.05 \leq f < 8$	$-9.5 + 0.37 * (f)$
$8 \leq f < 14.1$	$-4.75 + 7.4 * \log_{10}(f/14)$

Table 5: FDR SCC11 and SCC22

Range (GHz)	Max Value (dB)
$.200 \leq f < 14.1$	-2

Table 6: FDR SDC11 and SDC22

Range (GHz)	Max Value (dB)
$0.01 \leq f < 12.89$	$-22 + 20 * (f/25.78)$
$12.89 \leq f < 14.1$	$-15 + 6 * (f/25.78)$

Table 7: FDR ICN

Range (GHz)	Max Value (mV)
$3 \leq IL \leq 7.65$	9
$7.65 < IL \leq 15.0$	$12.75 - 0.49 * IL$

Table 8: FDR ILD_{rms} and ICMCN

Measurement	Max Value
ILD_{rms}	0.41 dB _{rms}
ICMCN	40 mV

Appendix C – EDR S Parameter Requirements

Table 9: EDR Insertion Loss

Description	Min Value	Max Value	Unit
Maximum insertion loss at 12.89 GHz	-	16.74	dB
Maximum fitted insertion loss coefficient a_0	-0.75	0.5	dB
Maximum fitted insertion loss coefficient a_1	0	17.96	dB
Maximum fitted insertion loss coefficient a_2	0	10.25	dB
Maximum fitted insertion loss coefficient a_4	0	7.91	dB

Table 10: EDR Insertion Loss Deviation (ILD)

Frequency (GHz)	Min Value	Max Value	Unit
$0.05 \leq f < 5.0$	-0.75	0.75	dB
$5.0 \leq f < 15.5$	$-0.26*(f-5.0)-0.75$	$0.26*(f-5.0)+0.75$	dB
$15.5 \leq f \leq 19.5$	-3.5	3.5	dB

Table 11: EDR SDD11 and SDD22

Range (GHz)	Max Value (dB)
$0.05 \leq f < 8$	$-9.5 + 0.37 * (f)$
$8 \leq f \leq 26$	$-4.75 + 7.4 * \log_{10}(f/14)$

Table 12: EDR SCC11 and SCC22

Range (GHz)	Max Value (dB)
$0.05 \leq f < 26$	-2

Table 13: EDR SDC11 and SDC22

Range (GHz)	Max Value (dB)
$0.01 \leq f < 12.89$	$-22 + 20 * (f/25.78)$
$12.89 \leq f < 26$	$-15 + 6 * (f/25.78)$

Table 14: EDR ICN

Range (GHz)	Max Value (mV)
$3 \leq IL \leq 7.65$	9
$7.65 < IL \leq 26.0$	$12.75 - 0.49 * IL$

Table 15: EDR ILD_{rms} and ICMCN

Measurement	Max Value
ILD_{rms}	0.41 dB _{rms}
ICMCN	60 mV

Appendix D – PNA Calibration

Calibrations is performed using the Keysight Electronic Calibration Module (ECal) Model N4691B or N4692A. Calibration must be performed **after every power cycle** or as needed. After plugging the ECal into a USB port on the PNA, please wait until the WAIT light goes out and the green READY light appears.

1) In the PLTS software, click File → New

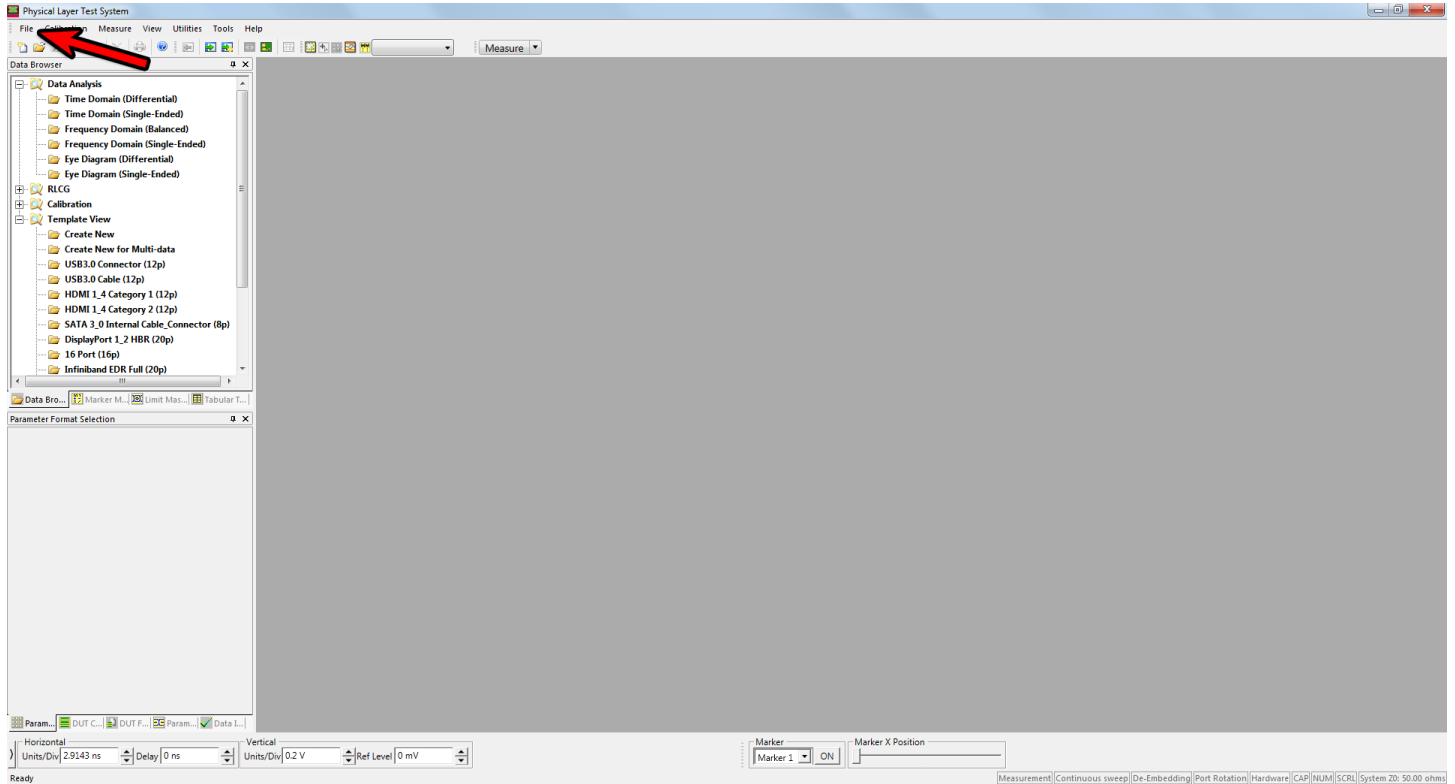


Figure 18 – PLTS new measurement

2) Select New Measurement, then click Next

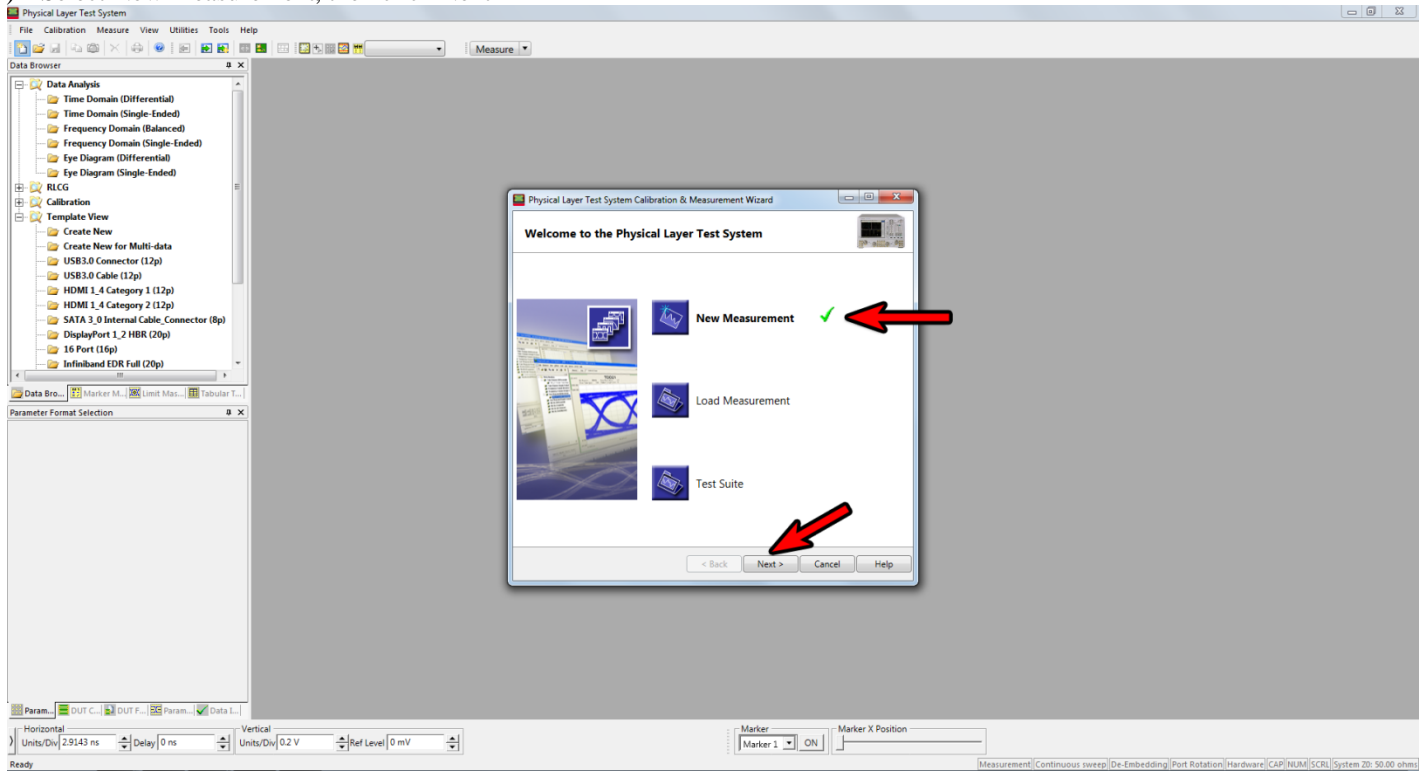


Figure 19 - PLTS measurement wizard

3) Click Edit under DUT Configuration section

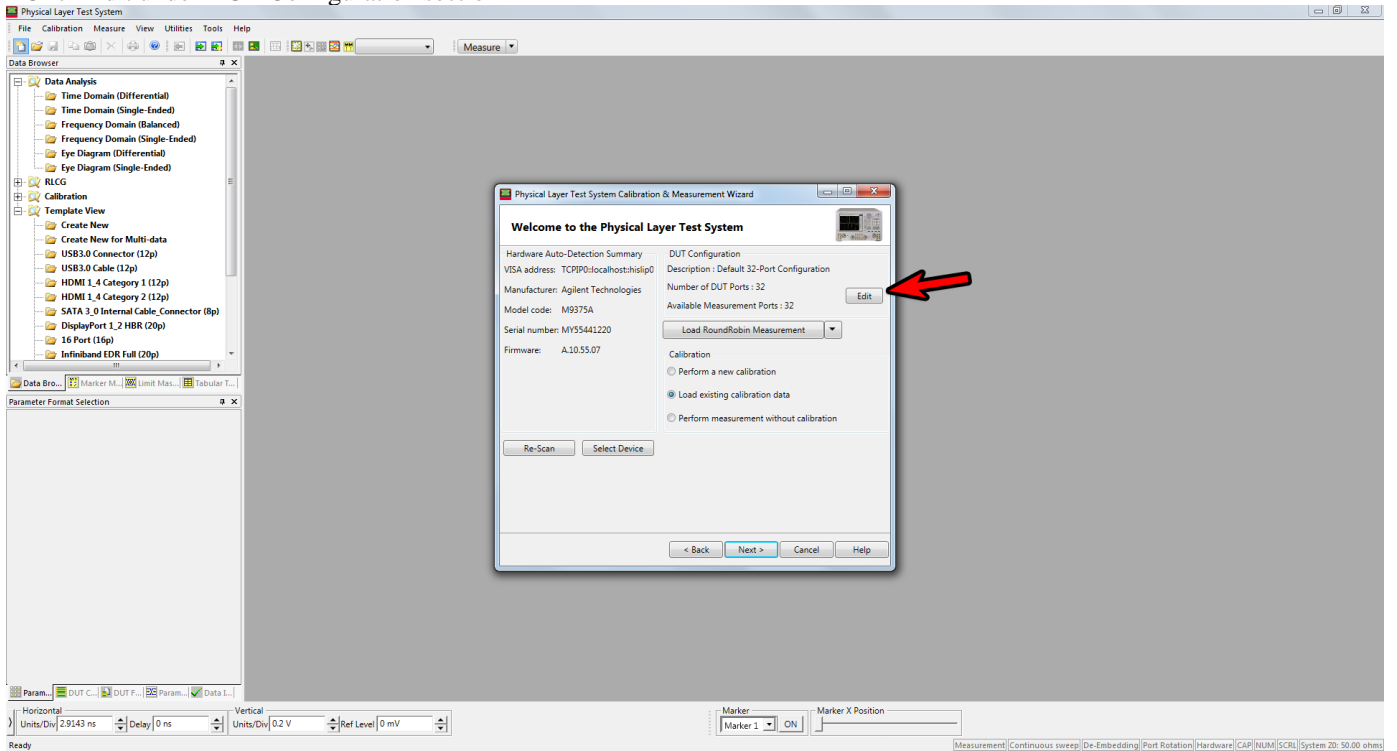


Figure 20 - PLTS select DUT configuration

Load an existing DUT configuration file by pressing the Load button and click OK. If a DUT configuration has not already been set up, refer to

- 6)
- 7) Keep the default configuration and click Next.

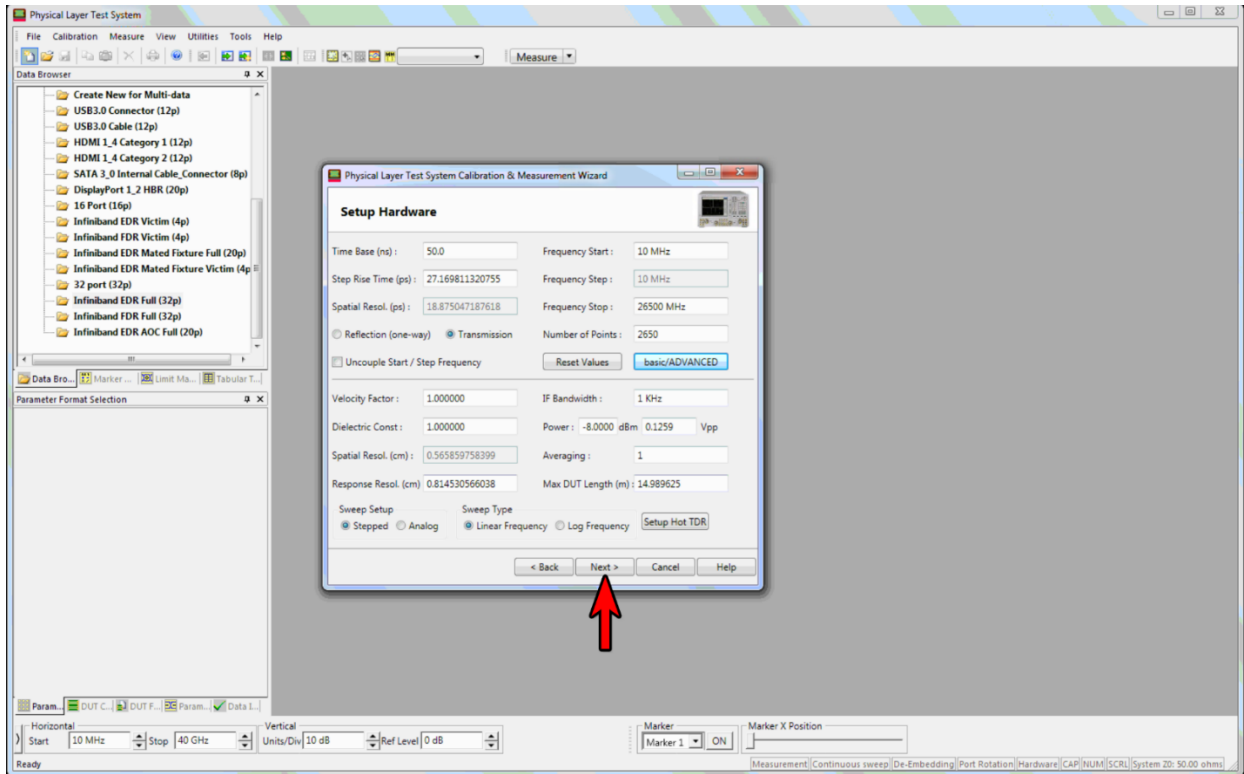


Figure 23 - PLTS default hardware setup

- 8) Select the model of the ECal unit being used in the Select Cal Kit drop down menu and then click the Apply to All Ports button.

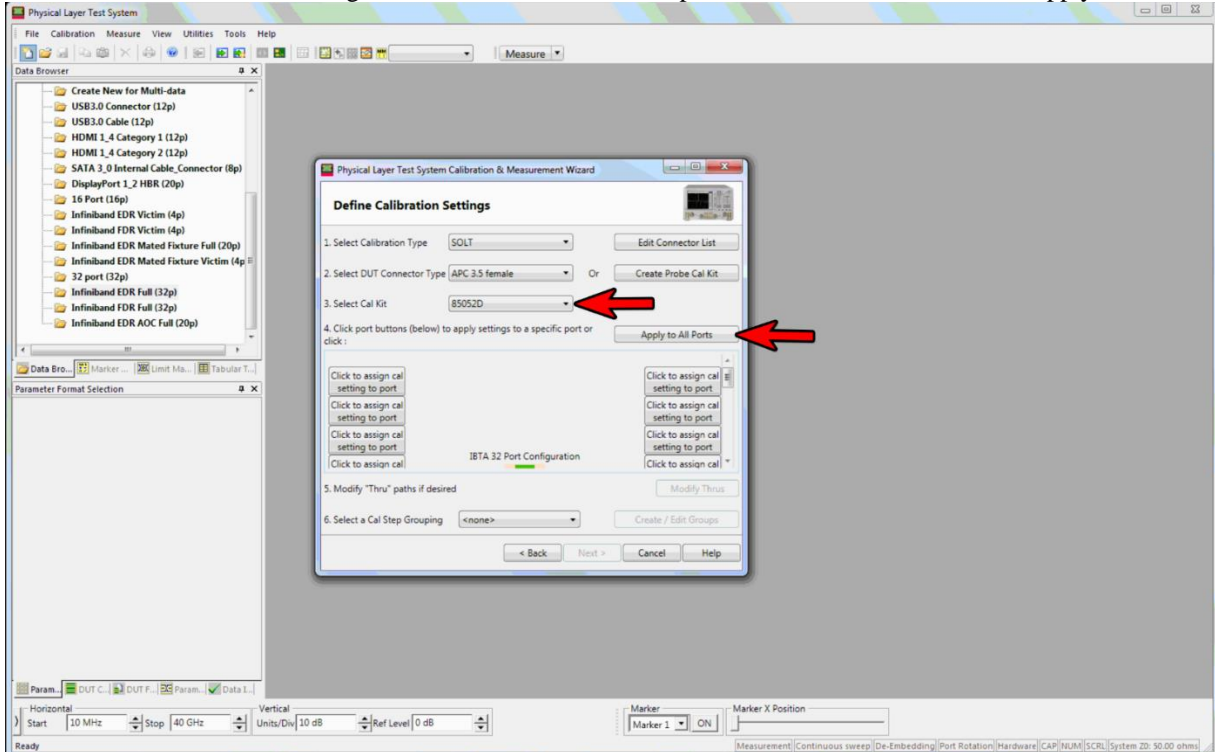


Figure 24 - PLTS Cal Kit setup

9) Once complete, click Next.

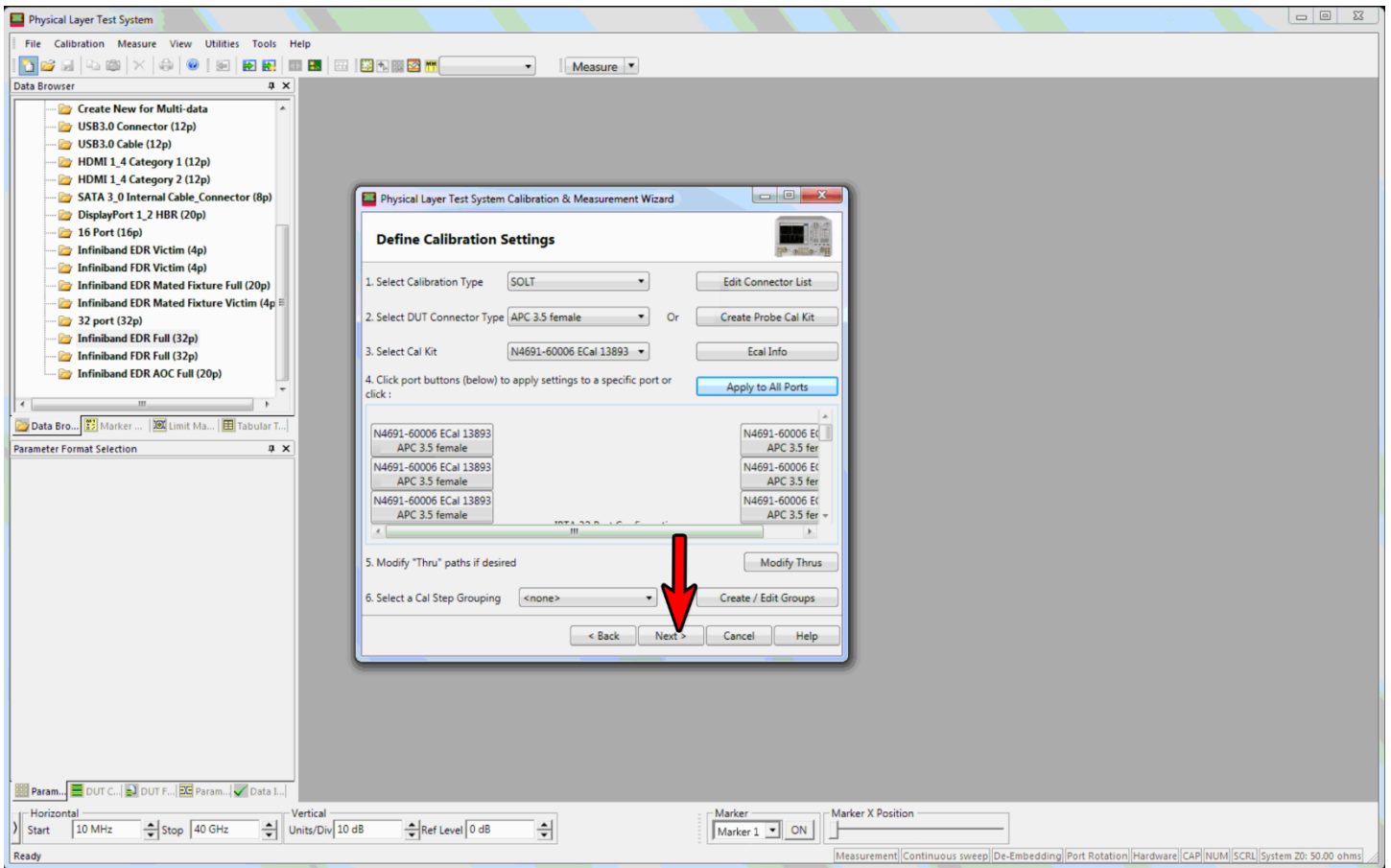


Figure 25 - PLTS finish calibration settings

- 10) Connect port 1 of the PNA to one of the ports on the ECal
- 11) Connect port 2 of the PNA to the other port on the ECal
- 12) Click the blue button to perform calibration of the two ports

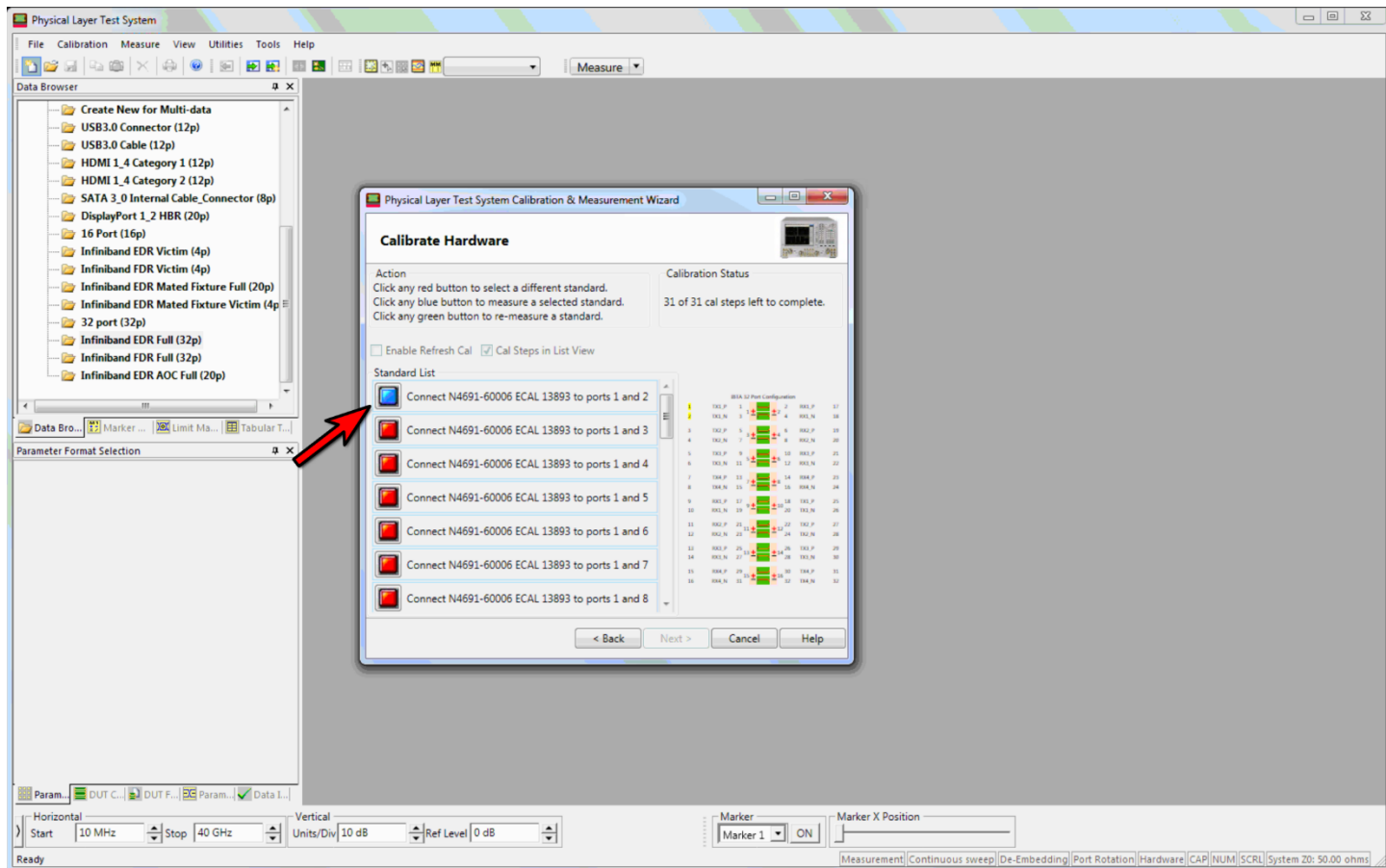


Figure 26 - PLTS calibration

- 13) When calibration of the ports is complete, the button will turn green and the next button will turn from red to blue.
- 14) Disconnect port 2 from the ECal and connect the next port, repeating the previous steps for ports 3-32 keeping port 1 connected at all times.
- 15) After all ports have been calibrated, all buttons will be green and the Next button will be enabled. Click Next.
- 16) Save the calibration using an easily identifiable name so that it can be loaded for future measurements without needing to recalibrate.

Appendix E – DUT Configuration

Physical Configuration

The default configuration of the PNA is to allocate the upper row of ports (odd numbered ports) to one device and the lower row of ports (even numbered ports) to the other. This mapping is shown graphically in Figure 29. It is often physically easier to change to the split 16 configuration in which ports 1-16 are allocated to one device and ports 17-32 are allocated to the other device.

Table 16 shows the mapping between the PNA ports and MCB connectors that should be connected to perform testing. Figure 27 shows the location of each port on the PNA (the cables are also usually physically labeled).

For passive cables: For consistency across all cables tested at a Plugfest, test the connector which has the worst lane in MCB-B and the other end in MCB-A. Additionally, the MCBs should **not** be powered for passive cable testing.

Table 16: 32 Port MCB Connection Layout

PNA Port	MCB	Connector	PNA Port	MCB	Connector
1	A	TX1P	17	B	RX1P
2	A	TX1N	18	B	RX1N
3	A	TX2P	19	B	RX2P
4	A	TX2N	20	B	RX2N
5	A	TX3P	21	B	RX3P
6	A	TX3N	22	B	RX3N
7	A	TX4P	23	B	RX4P
8	A	TX4N	24	B	RX4N
9	A	RX1P	25	B	TX1P
10	A	RX1N	26	B	TX1N
11	A	RX2P	27	B	TX2P
12	A	RX2N	28	B	TX2N
13	A	RX3P	29	B	TX3P
14	A	RX3N	30	B	TX3N
15	A	RX4P	31	B	TX4P
16	A	RX4N	32	B	TX4N

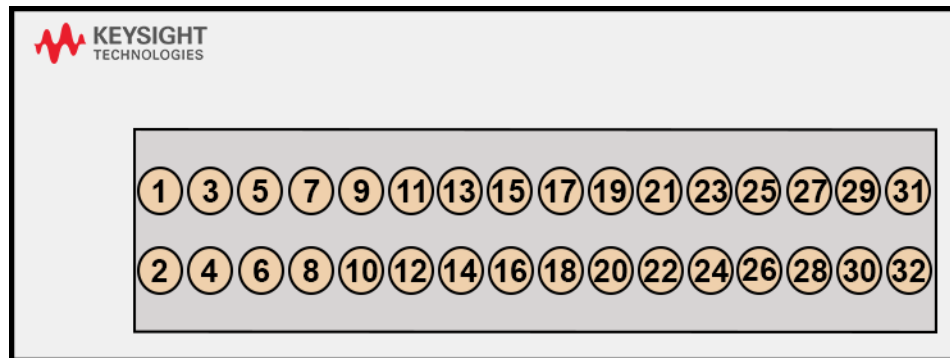


Figure 27 - PNA port layout

PLTS Configuration

PLTS must also be configured for the above setup. This is done in the DUT configuration step when creating a new measurement (refer to Procedure for Passive Cables for creating a new measurement). Instead of loading an existing configuration, you can configure a new one in the section shown in Figure 28.

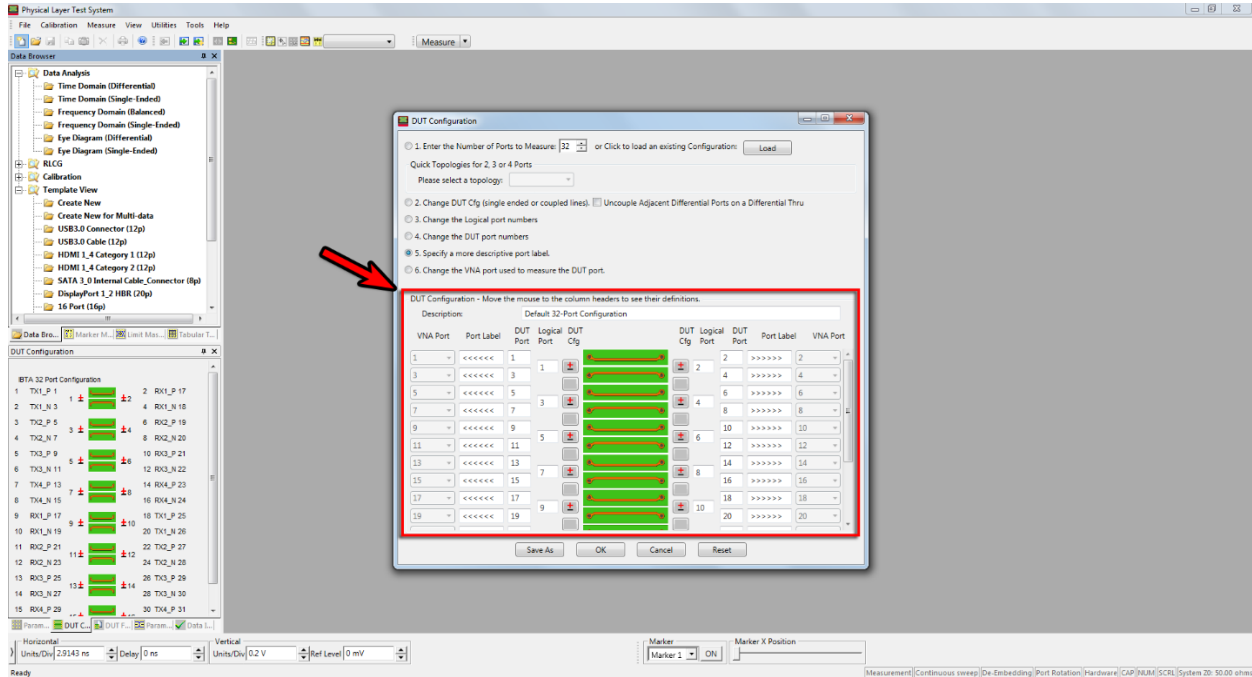


Figure 28 – PLTS DUT configuration

In the DUT configuration section, VNA port refers to the physical port on the PNA, port label is an arbitrary identifier for the port mapping, and DUT port refers to the port on the MCB. In the default configuration, there is a one to one mapping between the VNA port and the DUT port as shown in Figure 29. In order to make the split 16 configuration, the VNA ports should be changed to increase sequentially as shown in Figure 30. Figure 30 has also been labeled to show the mappings between the DUT port and their lane identifiers which matches the mappings described in Table 16.

VNA Port	Port Label	DUT Port	Logical Port	DUT Cfg		DUT Cfg	Logical Port	DUT Port	Port Label	VNA Port
1	<<<<<<	1	1	<input checked="" type="checkbox"/>		<input checked="" type="checkbox"/>	2	2	>>>>>>	2
3	<<<<<<	3		<input type="checkbox"/>		<input type="checkbox"/>		4	>>>>>>	4
5	<<<<<<	5	3	<input checked="" type="checkbox"/>		<input checked="" type="checkbox"/>	4	6	>>>>>>	6
7	<<<<<<	7		<input type="checkbox"/>		<input type="checkbox"/>		8	>>>>>>	8
9	<<<<<<	9	5	<input checked="" type="checkbox"/>		<input checked="" type="checkbox"/>	6	10	>>>>>>	10
11	<<<<<<	11		<input type="checkbox"/>		<input type="checkbox"/>		12	>>>>>>	12
13	<<<<<<	13	7	<input checked="" type="checkbox"/>		<input checked="" type="checkbox"/>	8	14	>>>>>>	14
15	<<<<<<	15		<input type="checkbox"/>		<input type="checkbox"/>		16	>>>>>>	16
17	<<<<<<	17	9	<input checked="" type="checkbox"/>		<input checked="" type="checkbox"/>	10	18	>>>>>>	18
19	<<<<<<	19		<input type="checkbox"/>		<input type="checkbox"/>		20	>>>>>>	20
21	<<<<<<	21	11	<input checked="" type="checkbox"/>		<input checked="" type="checkbox"/>	12	22	>>>>>>	22
23	<<<<<<	23		<input type="checkbox"/>		<input type="checkbox"/>		24	>>>>>>	24
25	<<<<<<	25	13	<input checked="" type="checkbox"/>		<input checked="" type="checkbox"/>	14	26	>>>>>>	26
27	<<<<<<	27		<input type="checkbox"/>		<input type="checkbox"/>		28	>>>>>>	28
29	<<<<<<	29	15	<input checked="" type="checkbox"/>		<input checked="" type="checkbox"/>	16	30	>>>>>>	30
31	<<<<<<	31		<input type="checkbox"/>		<input type="checkbox"/>		32	>>>>>>	32

Figure 29 - PLTS default DUT configuration

















VNA Port	Port Label	DUT Port	Logical Port	DUT Cfg	DUT Cfg	Logical Port	DUT Port	Port Label	VNA Port
1	TX1_P	1	1	+		+	2	RX1_P	17
2	TX1_N	3					4	RX1_N	18
3	TX2_P	5	3	+		+	6	RX2_P	19
4	TX2_N	7					8	RX2_N	20
5	TX3_P	9	5	+		+	10	RX3_P	21
6	TX3_N	11					12	RX3_N	22
7	TX4_P	13	7	+		+	14	RX4_P	23
8	TX4_N	15					16	RX4_N	24
9	RX1_P	17	9	+		+	18	TX1_P	25
10	RX1_N	19					20	TX1_N	26
11	RX2_P	21	11	+		+	22	TX2_P	27
12	RX2_N	23					24	TX2_N	28
13	RX3_P	25	13	+		+	26	TX3_P	29
14	RX3_N	27					28	TX3_N	30
15	RX4_P	29	15	+		+	30	TX4_P	31
16	RX4_N	31					32	TX4_N	32

Figure 30 - PLTS split 16 DUT configuration

Appendix F – QSFP-DD/OSFP Setup

There are 16 channels to measure with QSFP-DD cables so the procedure is slightly more complex and you must make four measurements.

The first two tests are similar to a regular QSFP cable where you are making a Thru measurement.

- 1) Attach the first 16 VNA cables to MCB1 (Tx1 to Tx8 – see Figure 33)
- 2) Attach the second 16 VNA cables to MCB2 (Rx1 to Rx8 – see Figure 33)
- 3) Run the usual VNA test procedure
- 4) Then flip the cable and run another thru test

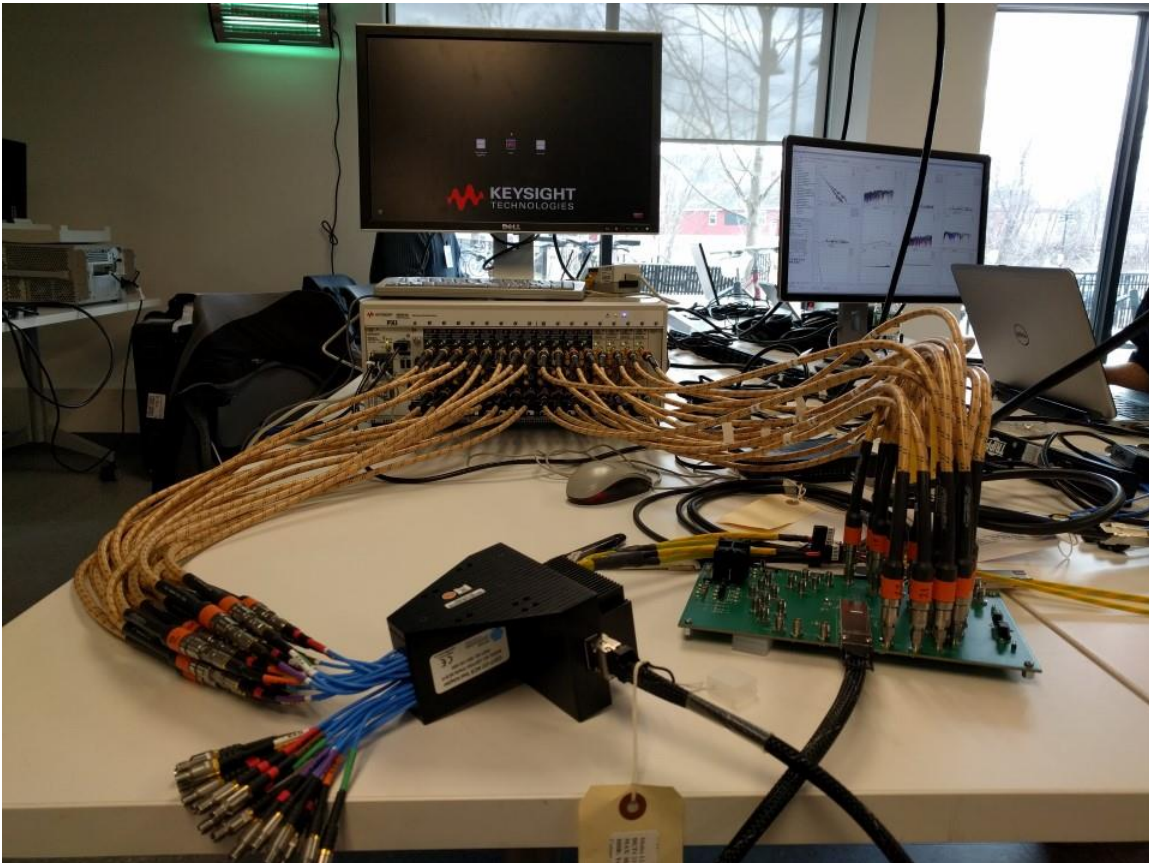


Figure 31 – QSFP-DD Setup for Thru Testing

The second set of tests is to measure crosstalk (ICN)

- 1) Attach the all 32 VNA cables to MCB1 (see figure 33 – Tx and Rx connections are the same, but on the same MCB)
- 2) Terminate all of the connectors on MCB2 with high quality 50 Ohm terminators (rated to at least 26 GHz)
- 3) Run the usual VNA test procedure
- 4) Then flip the cable and run another test

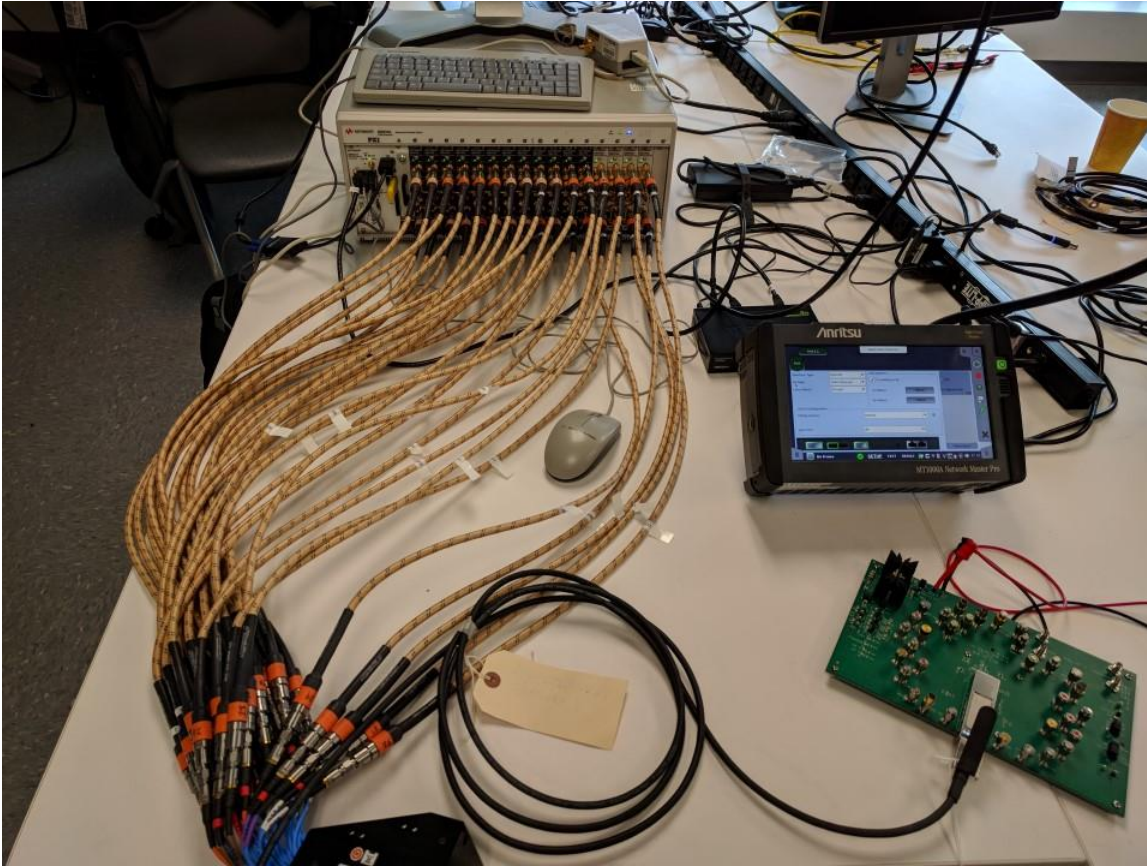


Figure 32 – QSFP-DD Setup for ICN Testing

VNA Connections

- 1) The port numbers highlighted in **Red** are the Physical Ports on the VNA
- 2) The port numbers highlighted in **Blue** are the Logical Single Ended Ports which represent what you see in the Touchstone files
- 3) The port numbers highlighted in **Green** are the Logical Differential Ports
- 4) OJ always connects the odd numbered physical ports on the VNA to the Positive connections on the MCB and the even numbered physical ports on the VNA to the Negative connections on the MCB

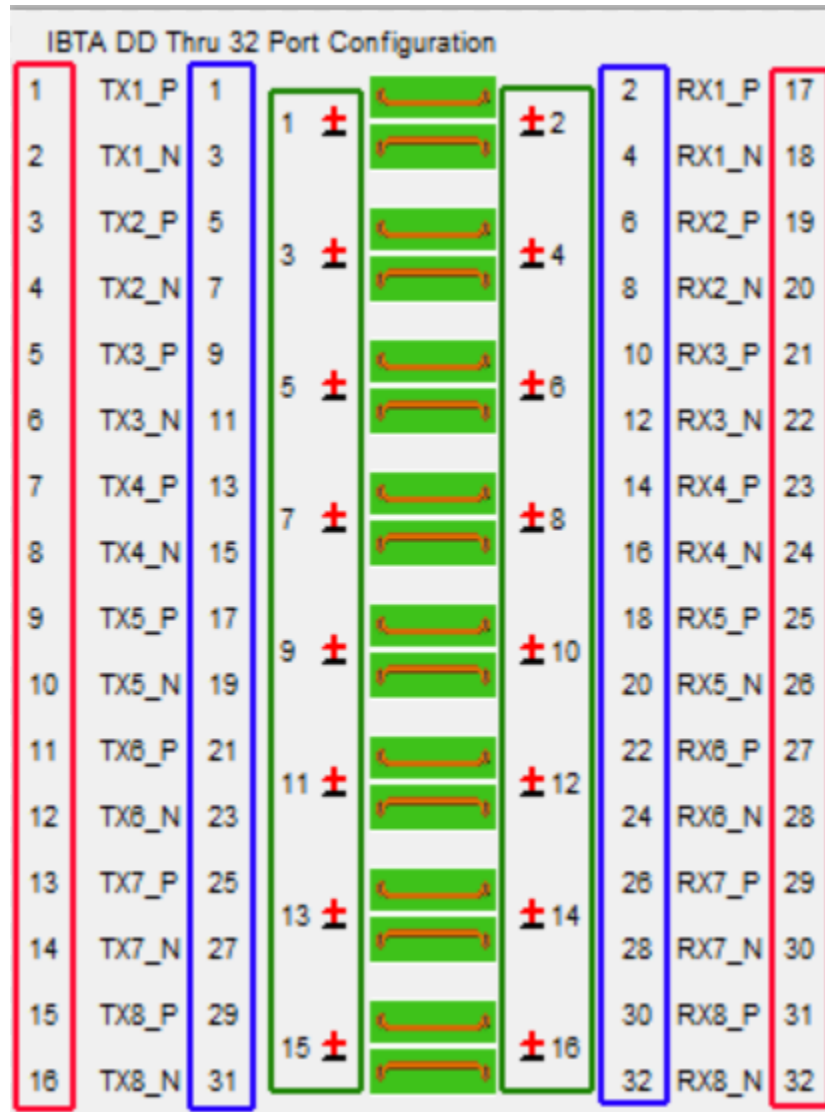


Figure 33 – QSFP-DD Connection Setup

Results

The plots shown for non-ICN tests can be used to determine pass or fail. All 12 plots are valid for passive cables. For AOC or passive equalized cables, only plots 2, 7 and 8 are valid.

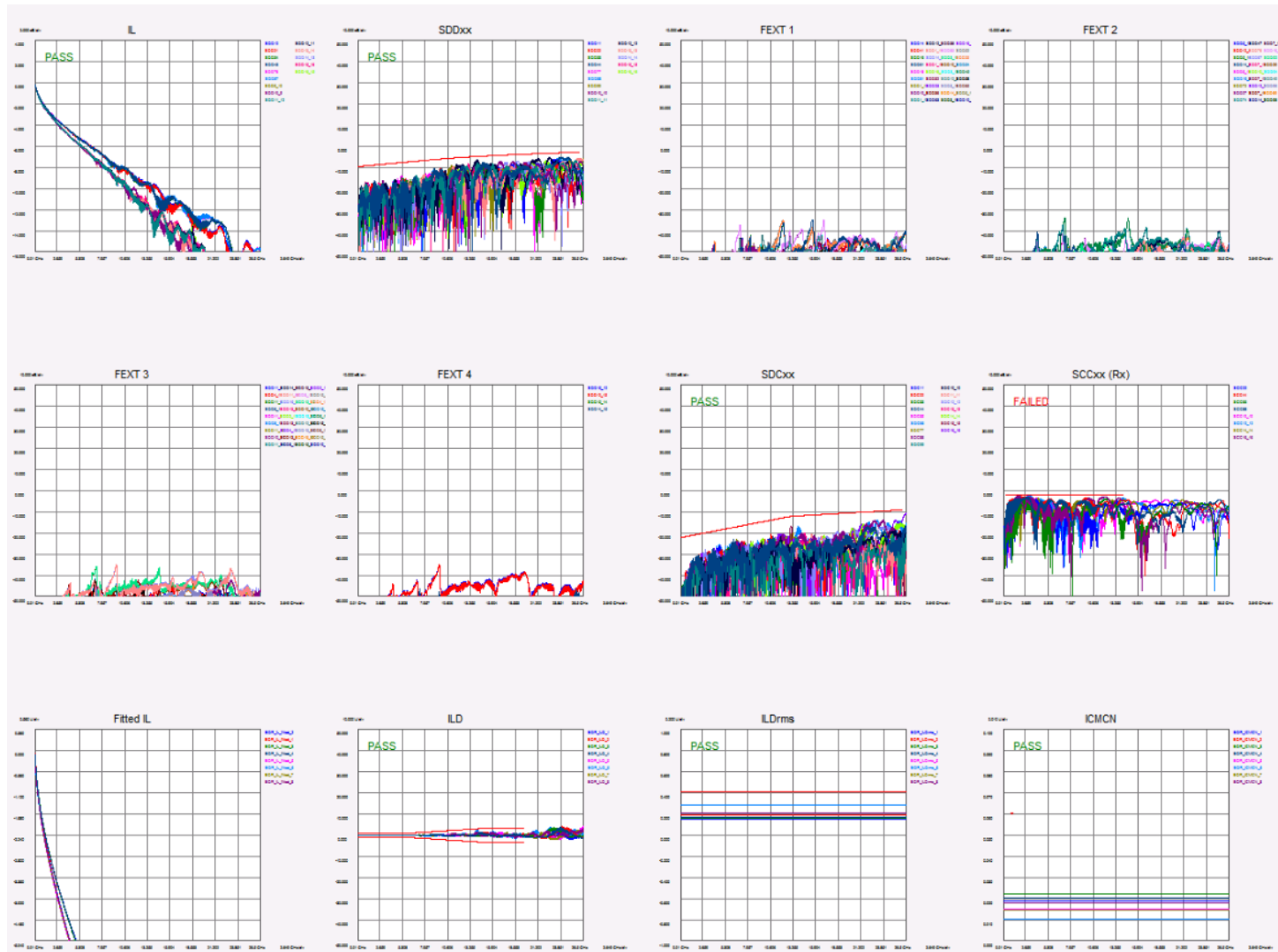


Figure 34 – Passive QSFP-DD Results Plots

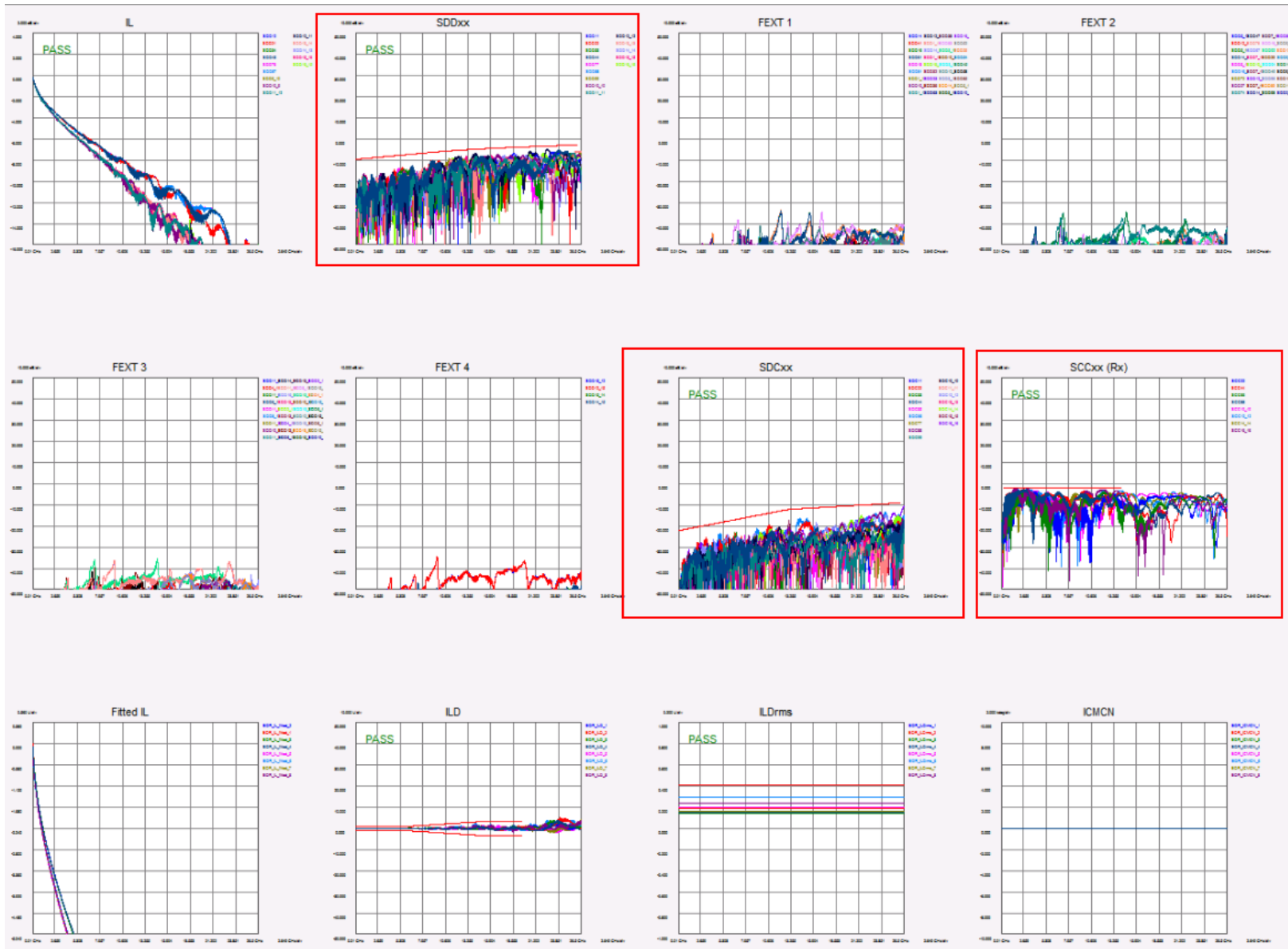


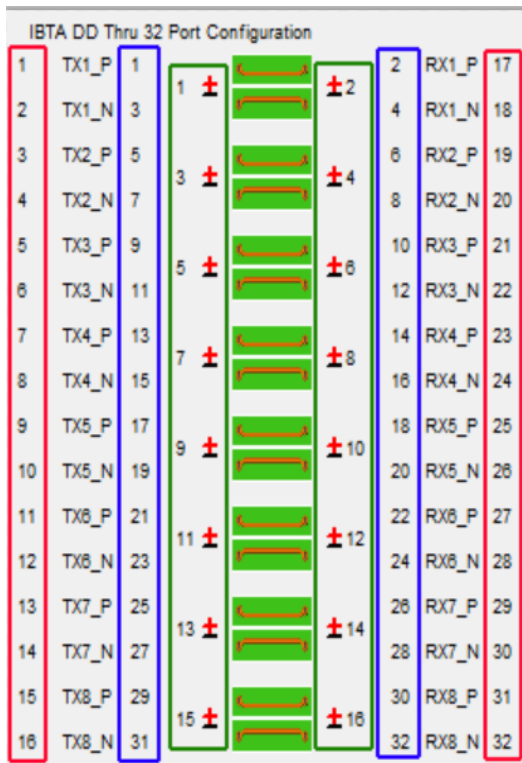
Figure 35 – AOC/Passive Equalized QSFP-DD Results Plots

Post Processing the QSFP DD data

- 1) In QSFP post processing we have 8 lanes we need to process and we take 4 transmit lanes from the MCB 1 and four transmit lanes from MCB2

VNA Port	Port Label	DUT Port	Logical Port	DUT Cfg	DUT Cfg	Logical Port	DUT Port	Port Label	VNA Port
1	TX1_P	1	1	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	2	2	RX1_P	17
2	TX1_N	3		<input type="checkbox"/>	<input type="checkbox"/>	4	4	RX1_N	18
3	TX2_P	5	3	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	6	6	RX2_P	19
4	TX2_N	7		<input type="checkbox"/>	<input type="checkbox"/>	8	8	RX2_N	20
5	TX3_P	9	5	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	10	10	RX3_P	21
6	TX3_N	11		<input type="checkbox"/>	<input type="checkbox"/>	12	12	RX3_N	22
7	TX4_P	13	7	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	14	14	RX4_P	23
8	TX4_N	15		<input type="checkbox"/>	<input type="checkbox"/>	16	16	RX4_N	24
9	RX1_P	17	9	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	18	18	TX1_P	25
10	RX1_N	19		<input type="checkbox"/>	<input type="checkbox"/>	20	20	TX1_N	26
11	RX2_P	21	11	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	22	22	TX2_P	27
12	RX2_N	23		<input type="checkbox"/>	<input type="checkbox"/>	24	24	TX2_N	28
13	RX3_P	25	13	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	26	26	TX3_P	29
14	RX3_N	27		<input type="checkbox"/>	<input type="checkbox"/>	28	28	TX3_N	30
15	RX4_P	29	15	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	30	30	TX4_P	31
16	RX4_N	31		<input type="checkbox"/>	<input type="checkbox"/>	32	32	TX4_N	32

- 2) In QSFP-DD (and OSFP) we need to analyze 16 lanes versus 8 and we take all 16 lanes from the left-hand side. Notice that all of the TX lanes are on the left.



- 3) QSFP-DD has 4 files
 - a) Two are thru files and one is tagged A and one is B
 - b) Two are ICN files and they are tagged NEXT with one tagged A and one is B
- 4) Therefore, there will be four s32p files to process when testing a QSFP-DD or OSFP cable. Here is what needs to be done in the MATLAB algorithm:
 - a) Process the **thru files**
 - i) In the first s32p take all that data from the TX lanes. No need to swap between 4 from one and 4 from the other.
 - ii) In the second s32p file, take all the data from the TX lanes as described in 3.a
 - b) Process the ICN files
 - i) TBD – this will require processing all the NEXT Files

This is the code for QSFP Passive Copper processing

```

% We added the elseif section at PF31 with OJ.
% The 1 1 terms are the Tx and 2 2 terms are the RX
% On the MCB and the way we connect them the first four lanes going from left to right    % are Tx to Rx
% The second four lanes going from left to right are Rx to Tx
elseif strcmp(tx_type, 'Passive')
    offset = (channel-1)*4;
    if channel <= 4
        s4p = snp2smp(s_data,Z0,[offset+1 offset+2 offset+3 offset+4],Z0);
    elseif channel > 4
        s4p = snp2smp(s_data,Z0,[offset+2 offset+1 offset+4 offset+3],Z0);
    end
else

```

For DD Thru I use this algorithm but increase the number of channels to 8

```
offset = (channel-1)*4;  
if channel <= 4  
    s4p = snp2smp(s_data,Z0,[offset+1 offset+2 offset+3 offset+4],Z0);
```

```
offset = (channel-1)*4;  
if channel <= 8 # this is the only change needed  
    s4p = snp2smp(s_data,Z0,[offset+1 offset+2 offset+3 offset+4],Z0);
```

Ethernet handles ICN differently. IB has one number. MDNEXT and MDFEXT has both and don't do a combined.

S-Parameter terminology

- 1) 2-1
 - a) Two is transmit and one is receiving.

Appendix G – Active Copper Cables

Active Copper cables must be powered on both ends. In PF33 we used the Agilent E3610A as shown below. They can be tested with one connection as a standard QSFP, but both ends need to be powered. The parameters that are measured should be the same as an AOC cable, with the addition of the input parameters for SDD and SDC.

