100G EDR and QSFP+ Cable Test Solutions

(IBTA, 100GbE, CEI)

DesignCon 2017

James Morgante
Anritsu Company

Anritsu
envision : ensure

Presenter Bio

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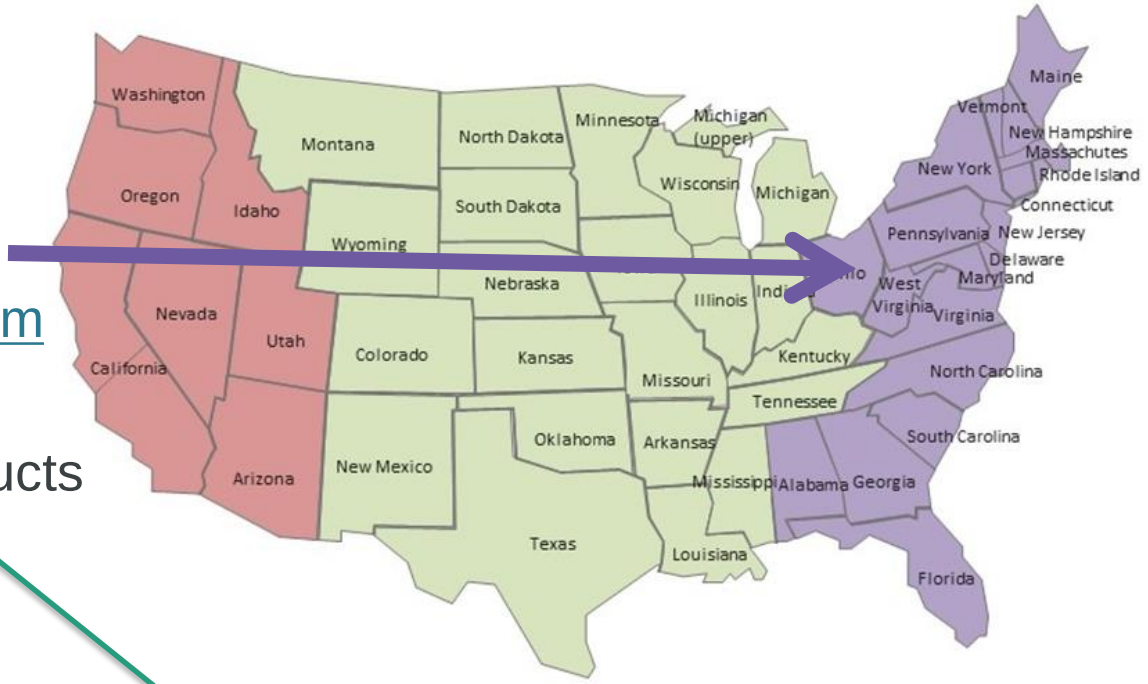


Wireline Digital / Optical Products

Career Experience

Product Development
RF, Mixed-Signal & Optical,
Application Engineering,
Test Engineering
Signal Integrity

MP1800A

Presentation Focus

- QSFP+ Cables / Modules
- Roadmap
- Active Time Domain (ATD) Test Objective
- EDR ATD Test System Overview
- Equipment requirements
- The calibration process
- The DUT test
- AOC final test
- InfiniBand & PAM4 (200G)

100G Modules & AOCs

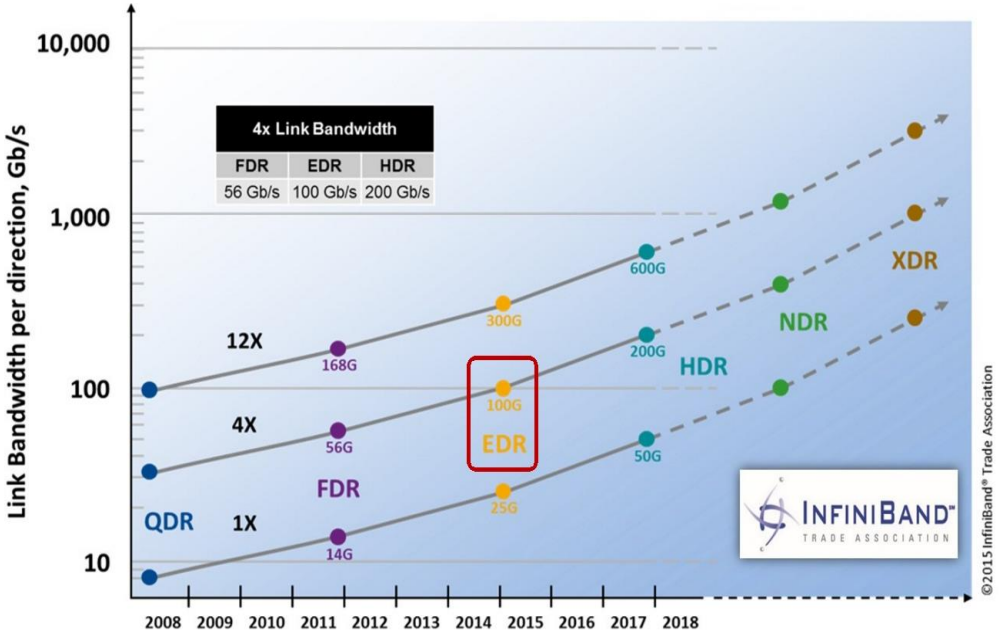
- QSFP+ Connectors.
- 4 x 25.78125 Gb/s Electrical Interface
- Data transfers rates over 100Gb/s
- Copper and Optical.
- Single & Multimode
- Multiple Fibers
  (IBTA EDR, 100GBase-SR4)
- Multiple Wavelengths
  (IEEE 100GBase-LR4)
- Single or Multiple connections per lane of traffic.

Ethernet Module

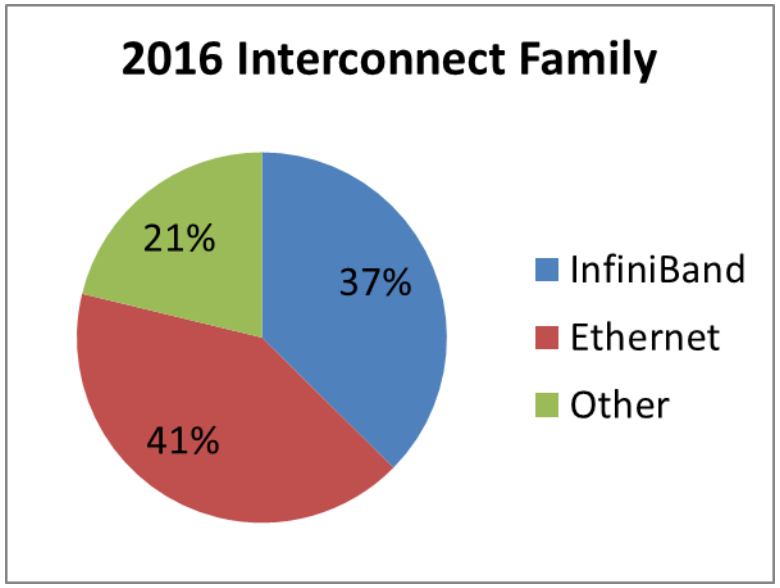
IBTA Interconnects

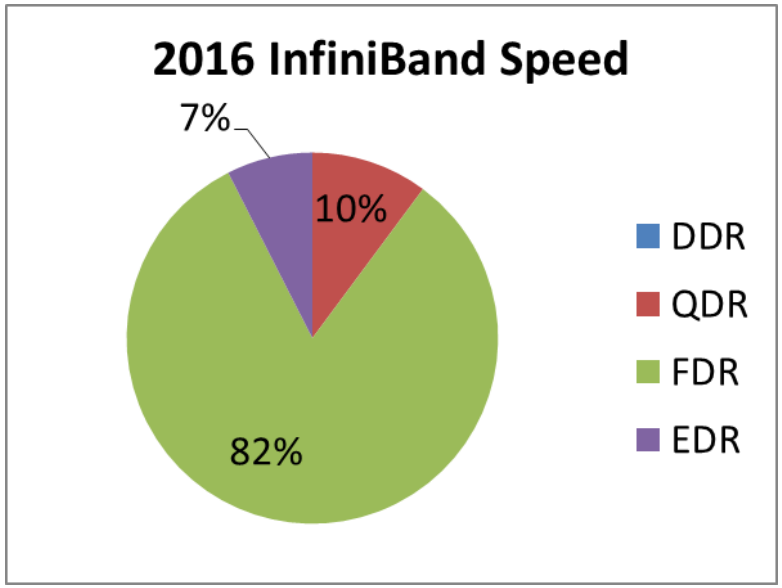
InfiniBand Data Rates		Baud Rate (Gbaud)	Per Lane (Gb/s)	x4 Lanes (Gb/s)	Modulation
Single Data Rate	SDR	2.50	2.50	10.00	NRZ
Double Data Rate	DDR	5.00	5.00	20.00	NRZ
Quad Data Rate	QDR	10.00	10.00	40.00	NRZ
Fourteen Data Rate	FDR	14.06	14.06	56.24	NRZ
Enhanced Data Rate	EDR	25.78	25.78	103.12	NRZ
High Data Rate	HDR	25.78	51.56	206.24	PAM4

InfiniBand Roadmap



http://infinibandta.org/content/pages.php?pg=technology_overview

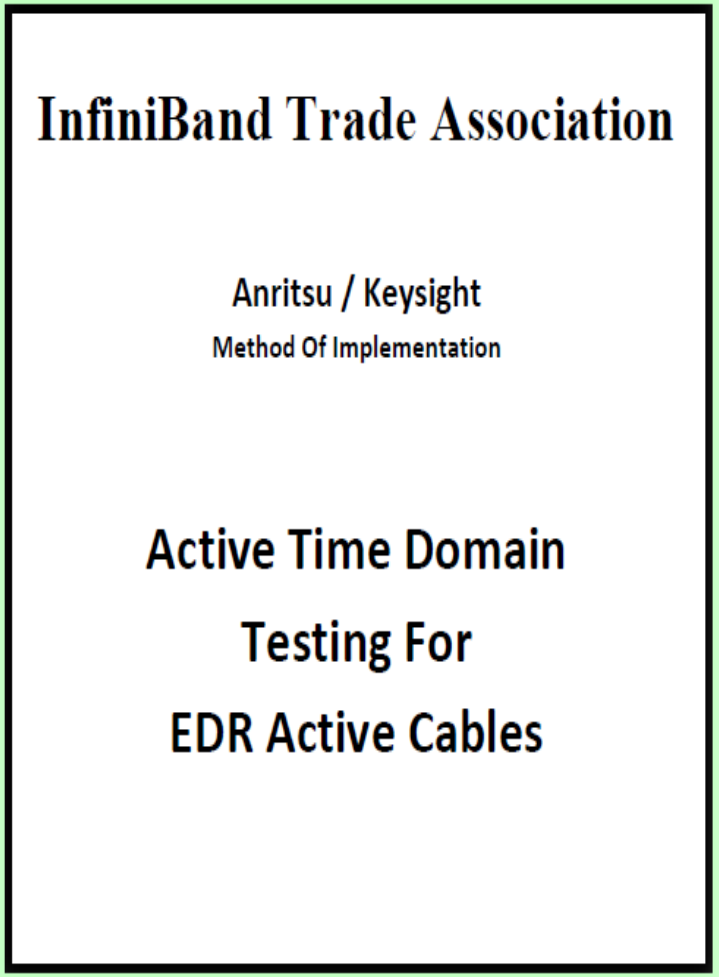




http://www.top500.org/lists/2016/11/

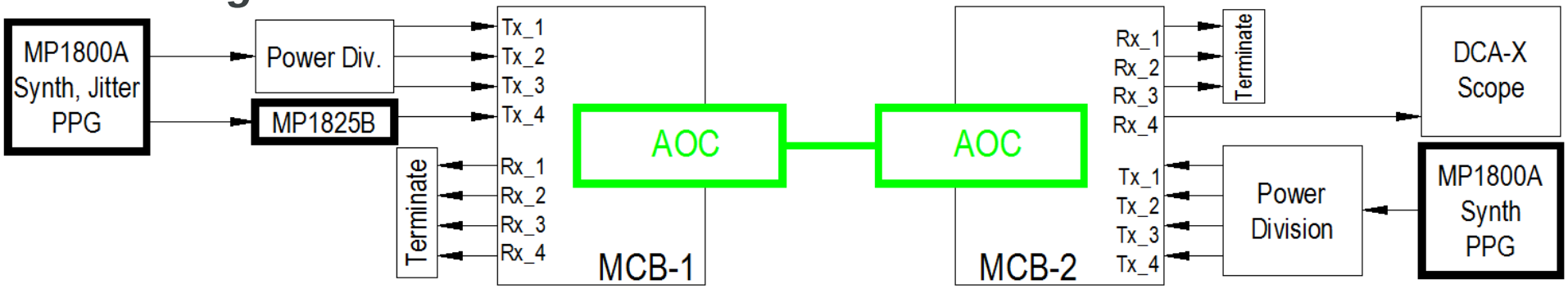
ATD (Stressed Receiver) Test Objective

- **Live Demo @ Anritsu Booth # 633**
- Stressed receiver sensitivity
- Output eye compliance
- Fully described in EDR MOI:
  https://cw.infinibandta.org/document/dl/7807
- Test methods used at IBTA Plugfests for EDR AOCs
- **Simplified** test approach.
- **4-Lane BER, 1-Lane Time Domain**

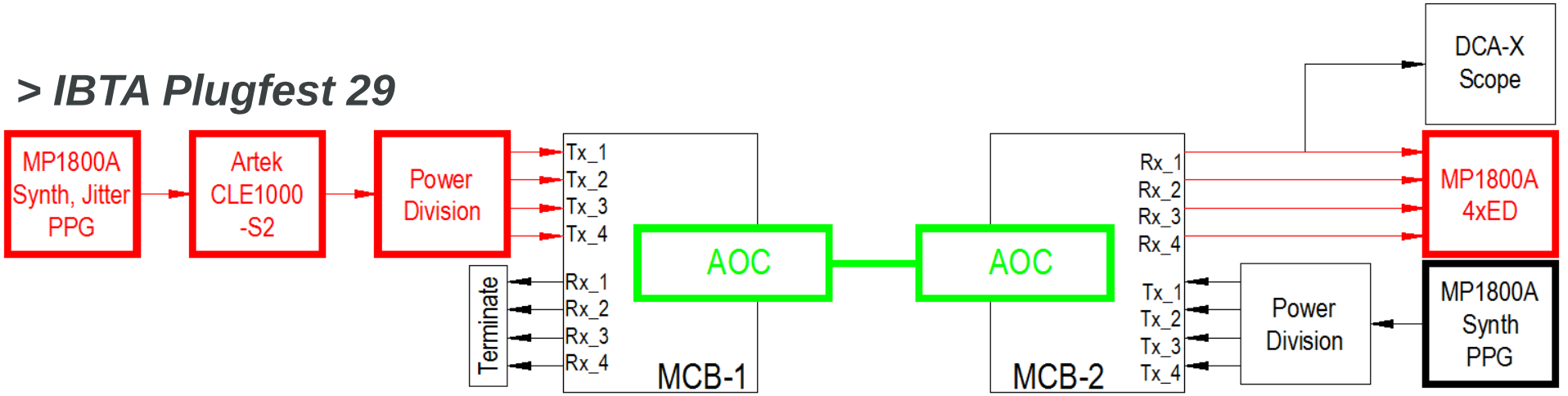


InfiniBand ATD Advancement

< *IBTA Plugfest 29*



> *IBTA Plugfest 29*



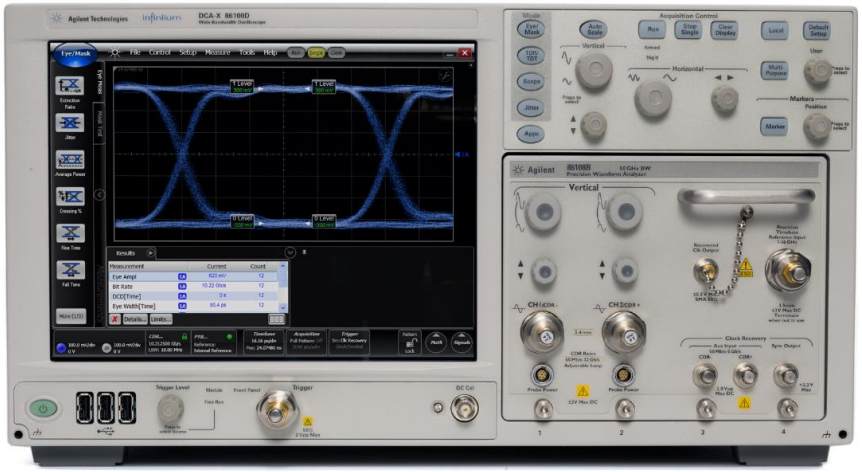
Changes:

- Adopted CAUI-4 Stressed Signal calibration methods described in 802.3bm Annex 83E.
- Calibration through a channel and usage of DCA-X CTLE function to emulate DUT CTLE.
- BER measurements to judge performance of DUT under stressed conditions.
- DUT CTLE to compensate for channel loss during test.

Principal Components

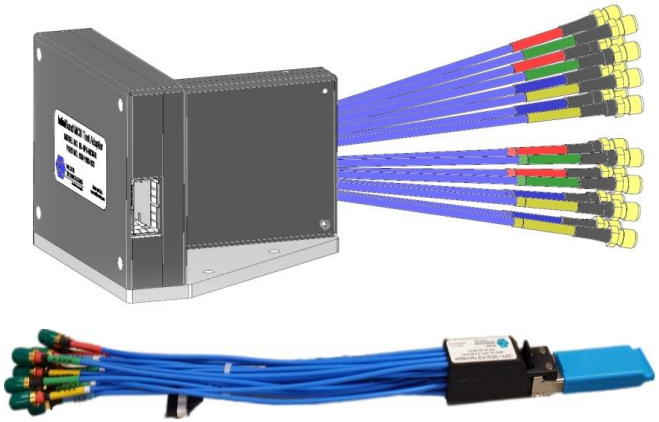
Multi-Port BERT

Anritsu MP1800A Shown



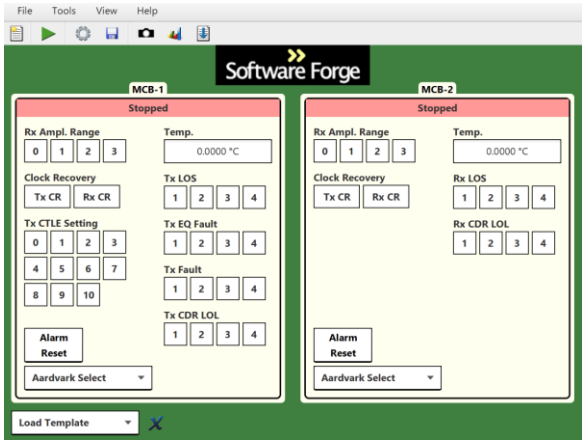
High BW Sampling Scope

Keysight DCA-X Shown



Compliance Fixtures

Wilder Technologies MCB /HCB



AOC Control

Software Forge

EEPROM Command Center

Variable ISI Channel

Artek CLE-1000-S2

Pattern Generators *(Anritsu MP1800A SQA)*

- ***Generating the right Stress Recipe***
- Multi-Channel for Forward & Reverse Traffic
- Comprehensive control of signal characteristics & applied jitter

Bitrate

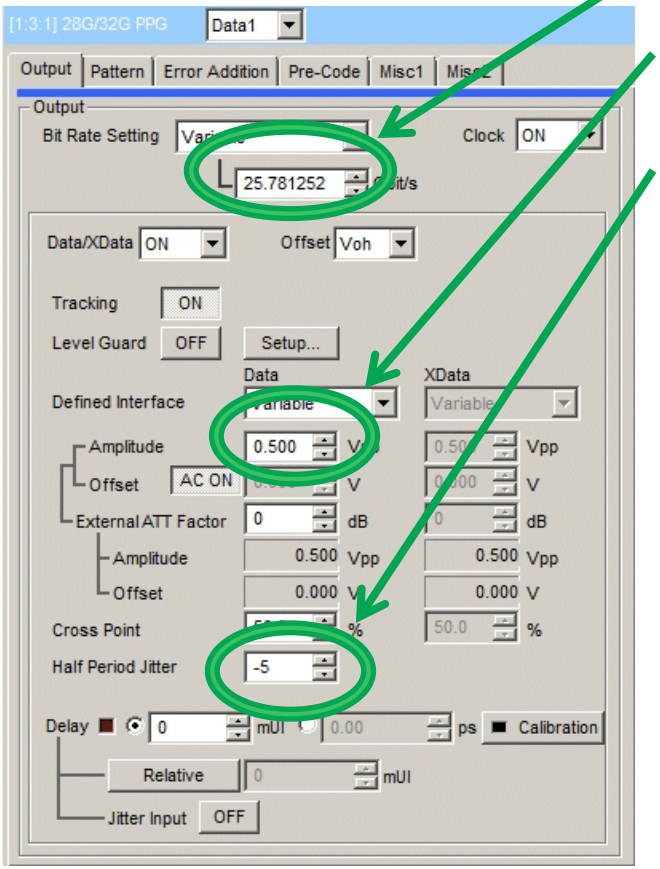
Amplitude

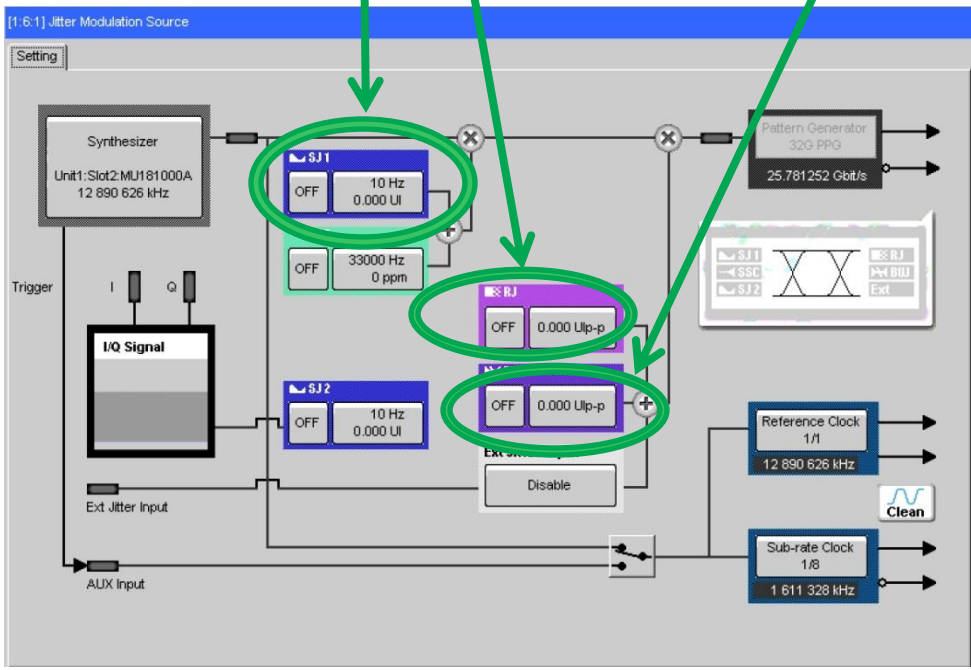
Even/Odd Jitter

Sinusoidal Jitter

Random Jitter

Bounded Uncorrelated Jitter





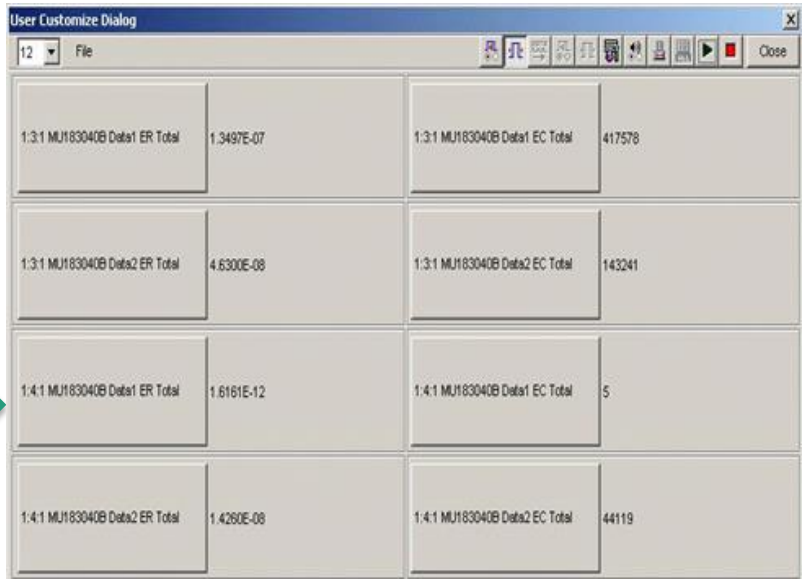
Measurement Equipment *(DCA-X 86100D, MP1800A SQA)*

Scope: (DCA-X 86100D / 86108B)

- ***For Victim Input Signal Cal & DUT Measurements***
- 2-Channel input for differential measurements
- ≈ 50 GHz Bandwidth
- Jitter Decomposition & Analysis Software
  - DDPWS, J2, J9 Jitter
- Eye Mask Compliance testing
  - Victim Input & Victim Output
- Precision Time Base
- Clock Recovery Capabilities
  - 1st order, LBW 10MHz,
  - 0 dB peaking, 20dB/decade roll/off
- CTLE needed for calibration

Error Detector: (MP1800A / MU183040B)

- ***Used for DUT Measurements***
- Multi-Channel to monitor all lanes.
- Measure BER



Test Fixtures *(Wilder Technologies)*

Actual figures from IBTA Spec

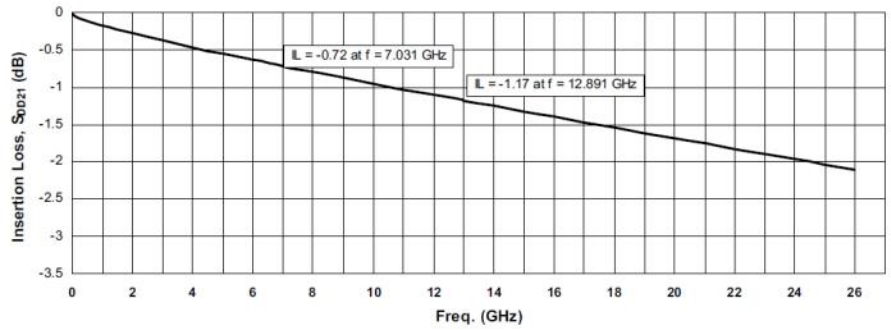


Figure 201 MCB trace pair reference through response

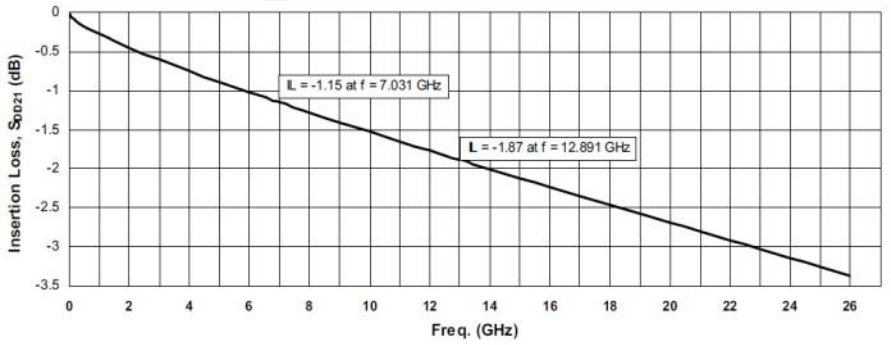


Figure 200 HCB trace pair reference through response

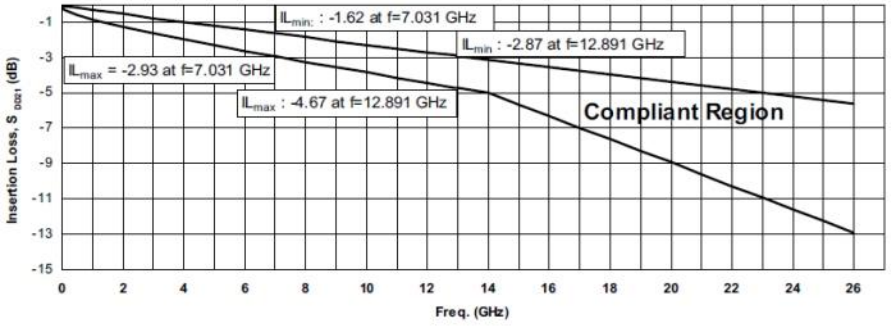
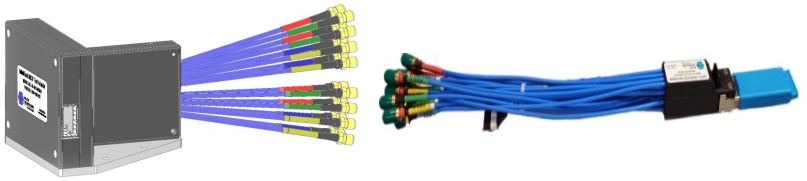


Figure 202 Mated HCB/MCB trace pair through response



Module Compliance Boards (MCB)

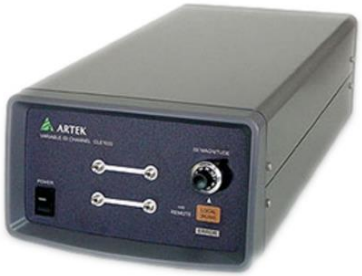
- Interface between QSFP cables and test equipment
- Drive transmit data into TX ports
- Measure received data from RX ports
- Supply power to the cable ends
- Low Speed interconnects
  - Cable programming
  - Reading registers

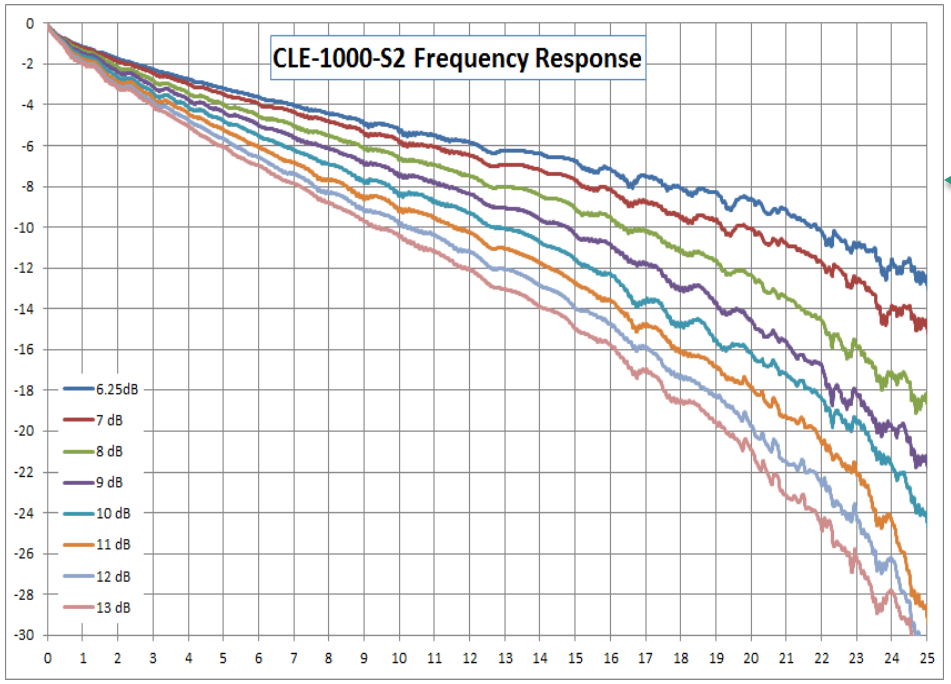
Host Compliance Board (HCB)

Break-out fixture to access QSFP ports

- Used only during ATD station calibration
- Inject signals into specific test points
- Measure signals at specific test points

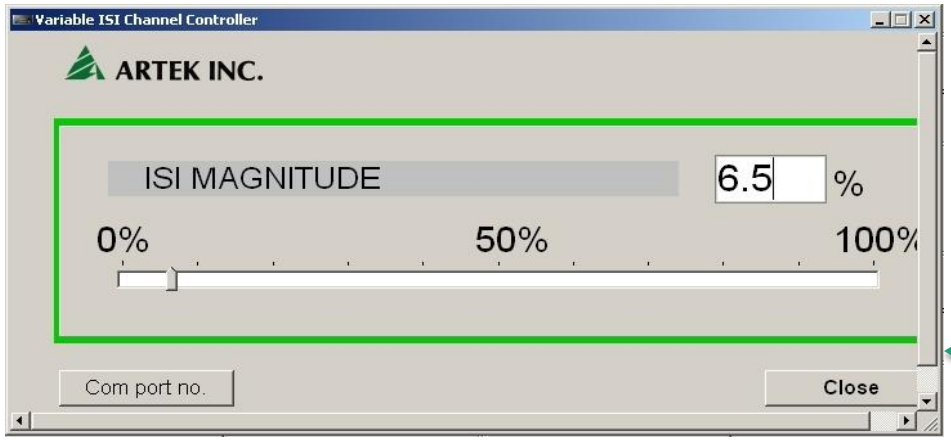
ISI Channel *(CLE-1000-S2 Ace Unitech / Artek)*





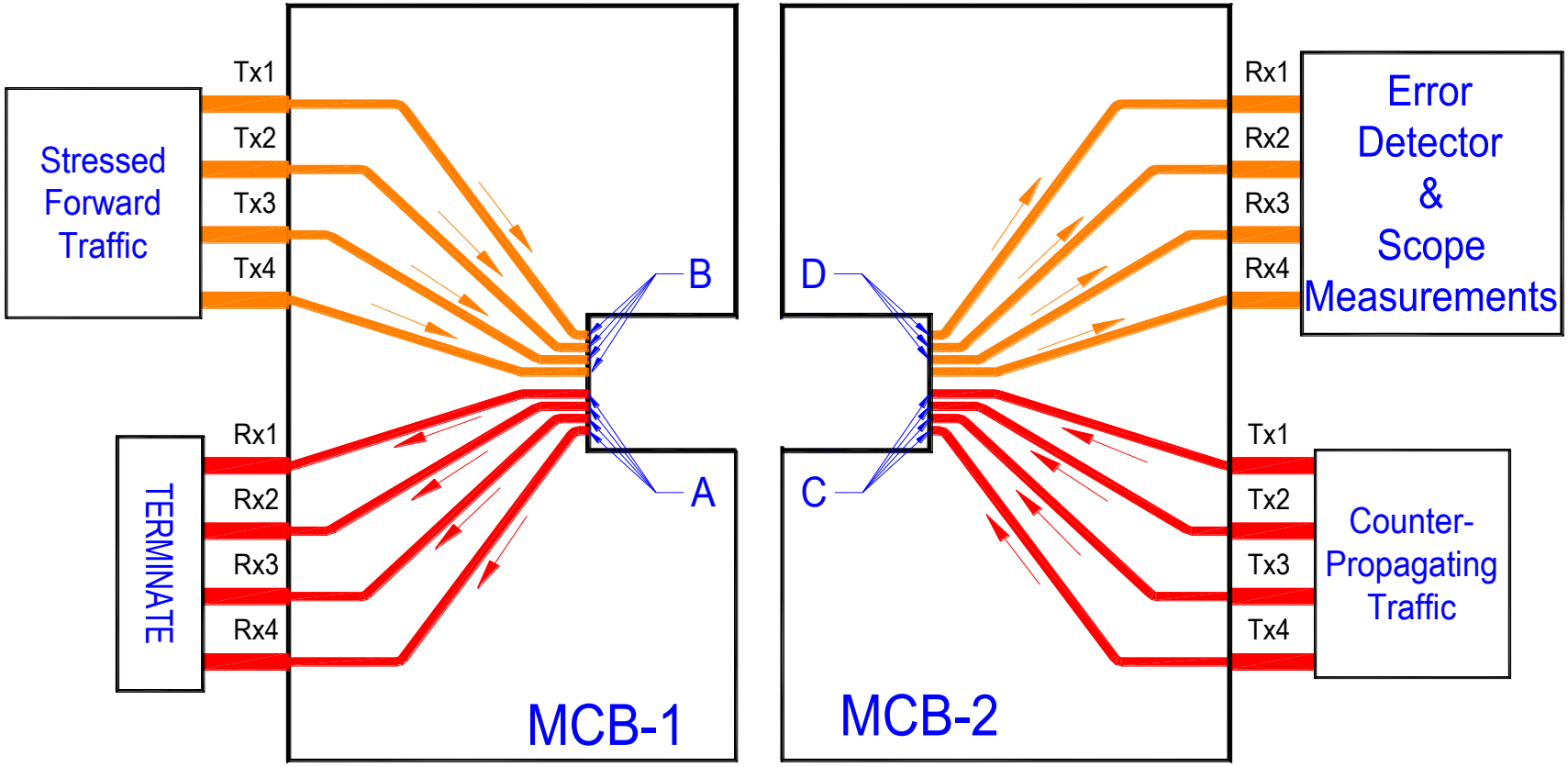
Plugfest Data

- Objective: Create Eye Closure normally produced by channel.
- Calibration requires a specified channel loss prior to DUT
- Affected signal at output of ISI channel is divided across the 4 forward lanes.
- DUT input signal is calibrated at output of channel (-10dB @ Nyquist) using Sampling Scope & CTLE to compensate.



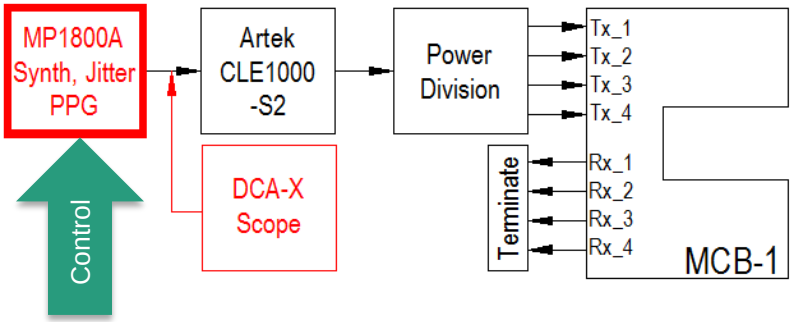
Simple control panel

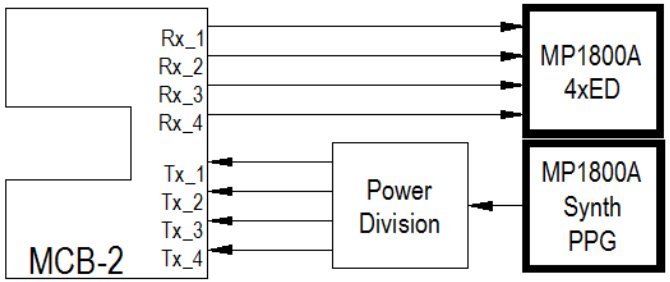
The EDR Calibration Process *Setting up equipment signals*



1. Set PPG Source Baseline Stresses (Forward Traffic)
2. Set MCB-1 counter-propagating aggressors **(A)** for crosstalk during forward traffic calibration.
3. Determine & set scope CTLE.
4. **Set MCB-1 forward traffic (B) in presence of counter-prop aggressors.**
5. Set MCB-2 aggressors **(C)** for crosstalk needed during DUT test.
6. Signal levels at point **(D)** are set after inserting DUT.

Calibration Step 1: *Setting Baseline PPG Stress*





- Set baseline Even-Odd Jitter, SJ, RJ, and BUJ as required by 802.3bm, Annex 83.
- SJ characteristics
  - AOC Clock Recovery stressor
  - .05UI @ 91MHz (used at PF29, 30)
- Backfill with BUJ to meet TJ requirement.
- Use DCA-X Scope to verify jitter components.

Excerpt: 802.3bm

Table 83E–9—Pattern generator jitter characteristics

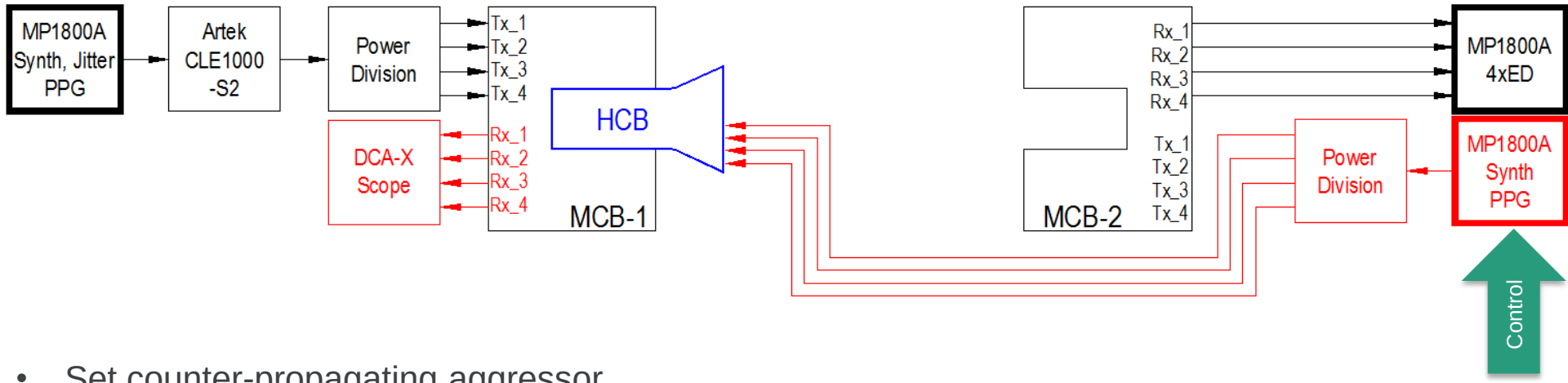
Parameter	Value
Total Jitter (pk-pk)[a]	0.28 UI
Random Jitter (pk-pk)[b]	0.15 UI
Max even-odd jitter (pk-pk)[c]	0.035 UI

[a]Total Jitter at BER of 10^{-15}
[b]Random Jitter at BER of 10^{-15}
[c]As defined in 92.8.3.8.1

Excerpt: 802.3bm *83E.3.4.1.1 Module stressed input test procedure*

be below the upper frequency limit of the pattern generator external modulator input. Random jitter and bounded uncorrelated jitter are added such that the output of the pattern generator approximates a jitter profile given in Table 83E–9. The target pattern generator 20% to 80% transition time in the module stressed

Calibration Step 2: *Setting Counter-Propagating FEXT Aggressors*



- Set counter-propagating aggressor signal levels to generate crosstalk for the forward traffic calibration.
- **Inject** aggressors into HCB Rx ports and **measure** with scope at corresponding MCB-1 Rx ports.

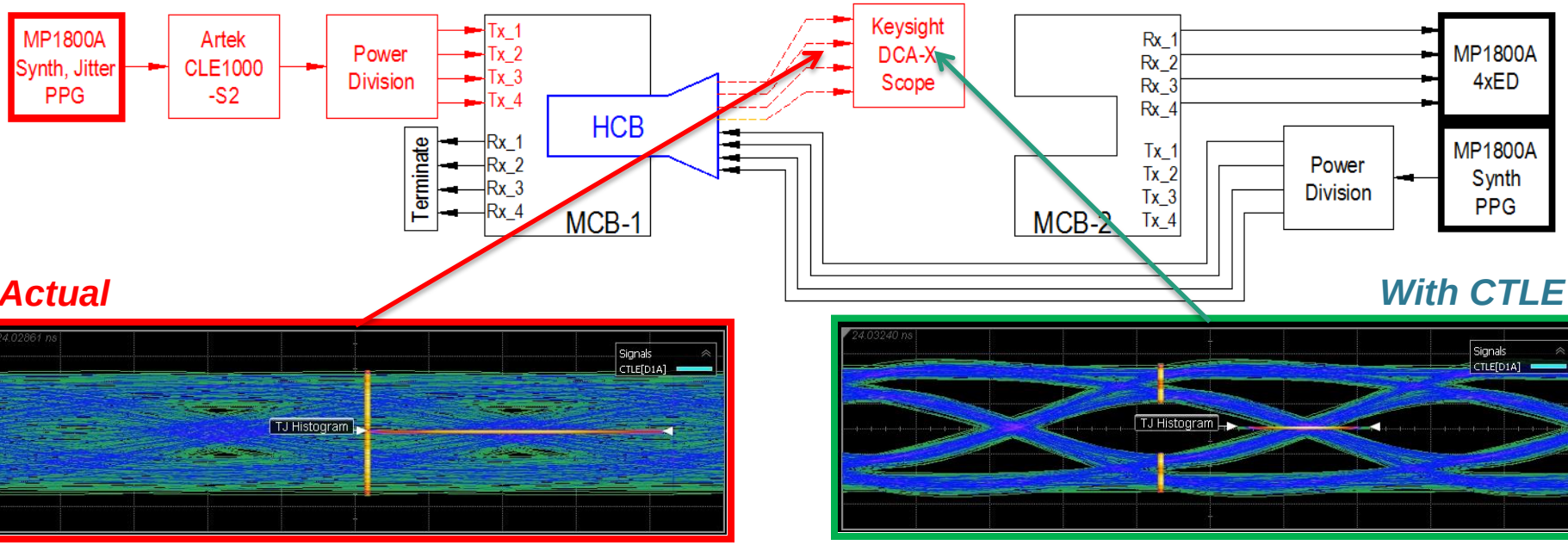
Excerpt: IBTA Spec v2r1_3_1.160825

Table 87 EDR limiting active cable input electrical specifications

Symbol	Parameter	Specification value(s)	Unit	Conditions
	Crosstalk signal Vpk-pk	+/- 5% (See Conditions)	mV	At TP6a. Co-propagating aggressors. Crosstalk signal Vpk-pk to match lane under test, to within +/- 20%.
	Crosstalk signal transition time, 20%-80%	17	ps	
	Crosstalk calibration signal Vpk-pk, each aggressor	450 +/- 10%	mV	At TP7a. Counter-propagating aggressors. Apply during crosstalk calibration only[a]
	Crosstalk calibration signal transition time, 20%-80%	17 +/- 3	ps	

Test Data:

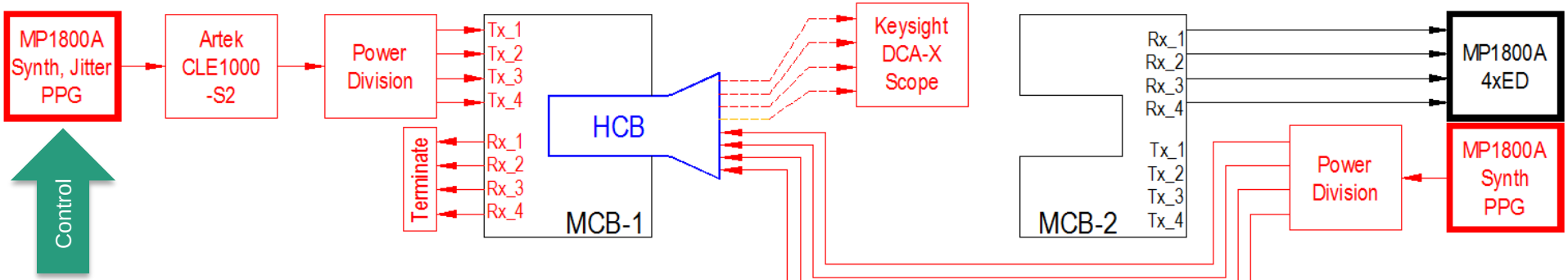
Calibration Step 3: *Determine Scope CTLE Setting*



- ISI Channel will significantly close the input eye.
- Goal: Use the scope's software CTLE to simulate the effect of the DUT's hardware CTLE.
- Target Eye Width and Height must be adjusted while applying software CTLE.
- The Optimal setting = setting with maximum product.

Scope CTLE	Eye Width (UI)	Eye Height (mV)	Product
2	N/A	N/A	N/A
3	N/A	N/A	N/A
4	0.418	70	29.26
5	0.512	86	44.03
6	0.536	102	54.67
7	0.54	111	59.94
8	0.512	114	58.37
9	0.51	100	51.00

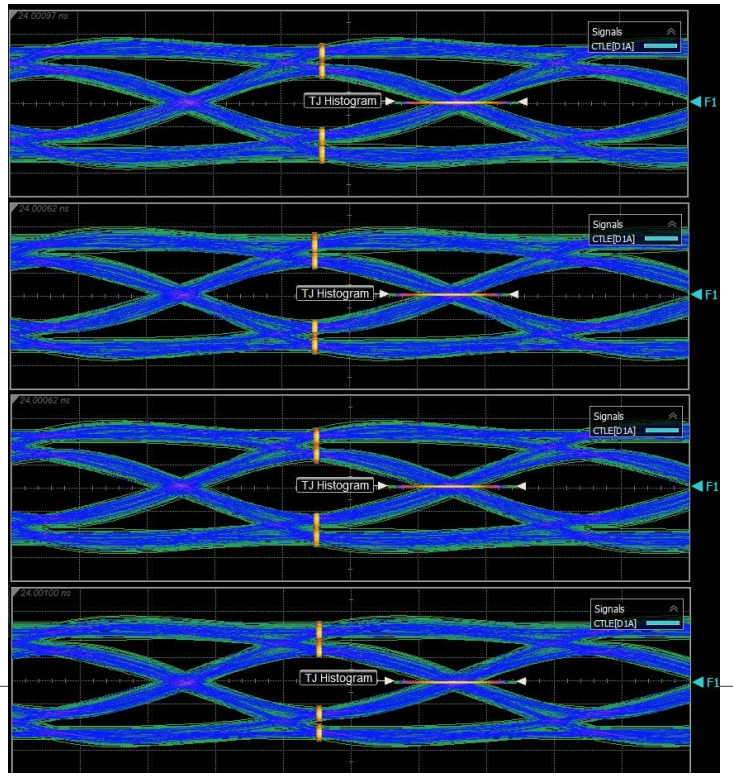
Calibration Step 4: *Setting Forward Traffic Stress*



- Send forward signal through ISI Channel & Divider.
- Counter- propagating aggressors turned on.
- Adjust the stressed forward signals.
- Adjust RJ to achieve Eye Width
- Adjust Amplitude to achieve Eye Height
- Set Eye Width & Eye Height targets per IBTA Spec
- ***Scope Measurement with CTLE, all channels***

Note: Eye is completely closed without CTLE

Test Data:



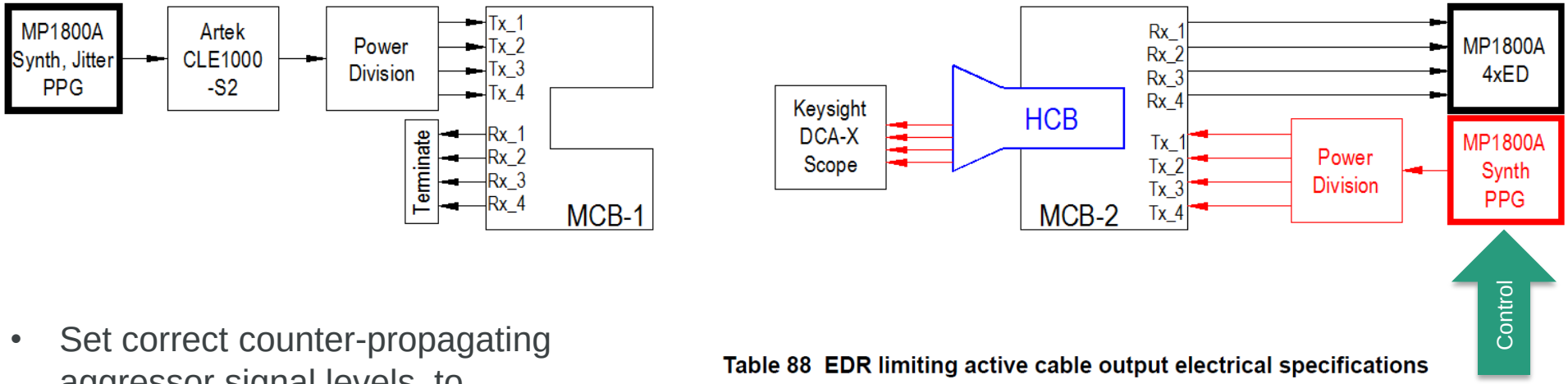
Excerpt: IBTA Spec v2r1_3_1.160825

EH15	Eye Height tolerance, at 1E-15	120		mV	
EW15	Eye Width tolerance, at 1E-15	0.53		UI	At TP6a, with TX CDR enabled
		0.71		UI	At TP6a, with TX CDR bypassed (i.e., disabled)

Excerpt: 802.3bm *83E.3.4.1.1 Module stressed input test procedure*

83E.4.2. Random jitter and the pattern generator output amplitude are adjusted (without exceeding the differential pk-pk input voltage tolerance specification as shown in Table 83E–7) to result in the eye height and eye width given in Table 83E–8 using the reference receiver with the setting of the CTLE that maximizes the product of eye height and eye width. For the low loss case, discrete frequency-dependent

Calibration Step 5: *Setting Counter-Propagating NEXT Aggressors*



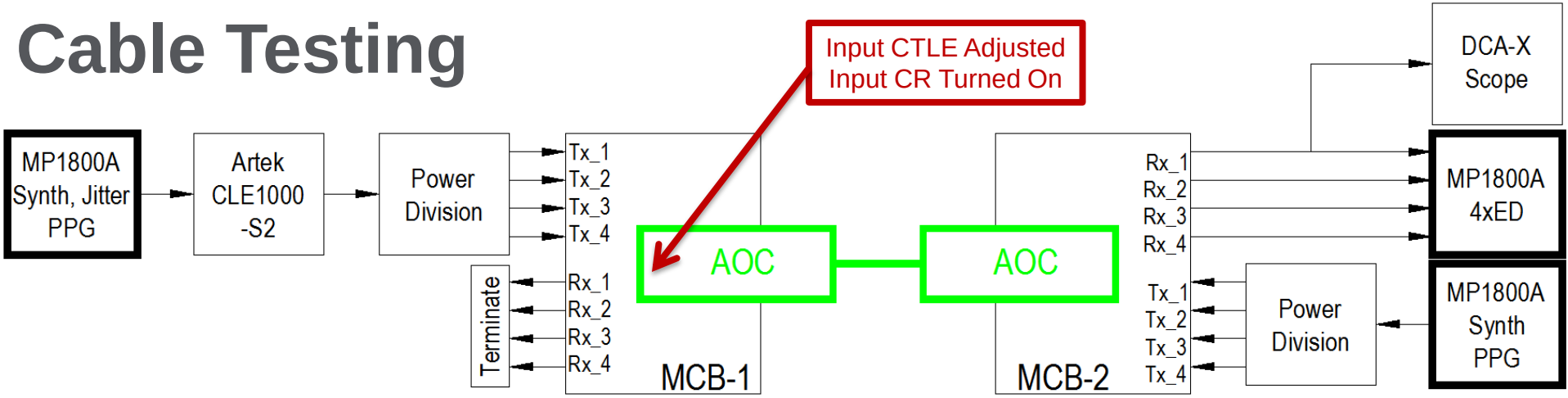
- Set correct counter-propagating aggressor signal levels to generate crosstalk for the DUT Test.
- **Inject** counter–propagating aggressor signals into MCB-2 Tx ports and **measure** with scope at corresponding HCB Tx ports.

Table 88 EDR limiting active cable output electrical specifications

Symbol	Parameter	Specification value(s)	Unit	Conditions
X	eye mask parameter, time; see Figure 86 on page 282	0.30	UI	Hit ratio=5E-5 with 100 Ohm load at TP7a (Note [a])
Y1, Y2	Diff. unsigned output voltage range 0 (required) range 1 (optional) range 2 (optional)	 50, 225 100, 350 150, 450	mV	
	Crosstalk signal Vpk-pk, each aggressor	700 +/- 10%	mV	At TP6a. Counter-propagating aggressors.[b]
	Crosstalk signal transition time, 20%-80%	17 +/- 3	ps	Transition time measured at this PRBS9 test pattern transition: 11111111**10**000011...

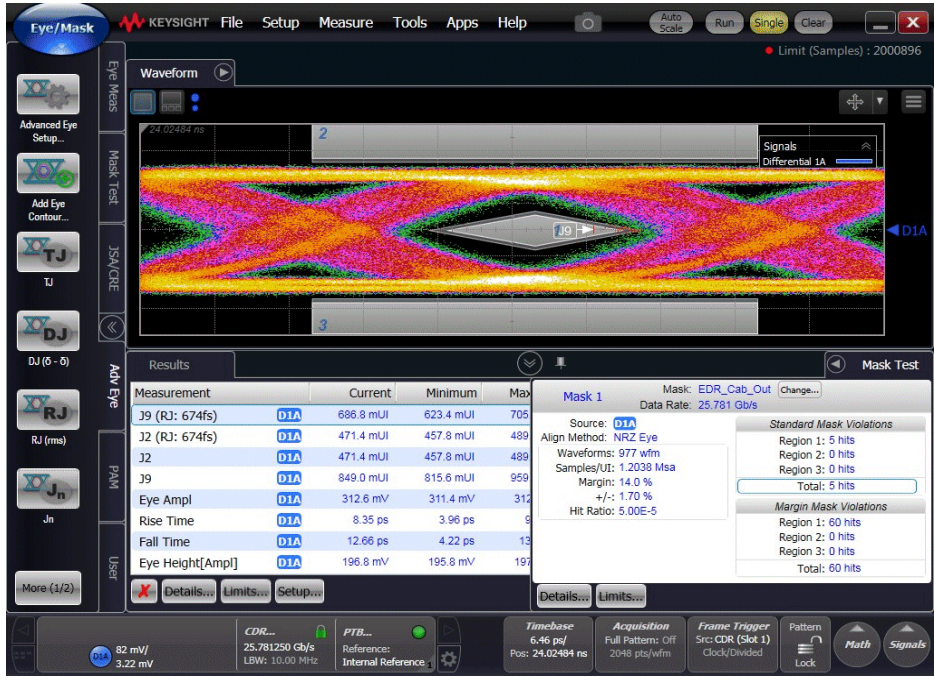
Test Data:

Cable Testing



BER Measurement:
Error Free, 2 minute gate, 4 channels

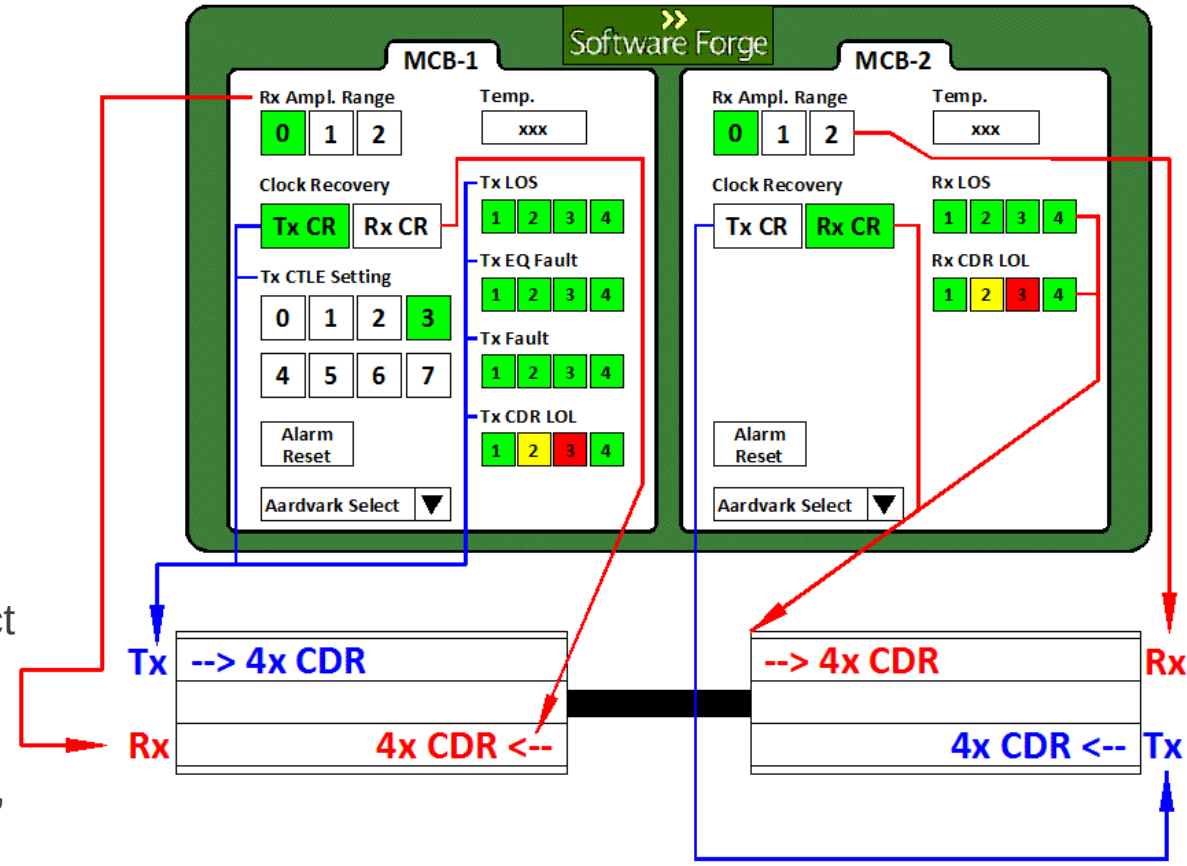
Scope Measurement:
J2, J9, Mask, Rise & Fall Times, 1 channel, 1M Samples



Scope judges Signal Integrity performance (Cable Output). ED judges BER (Cable Input).

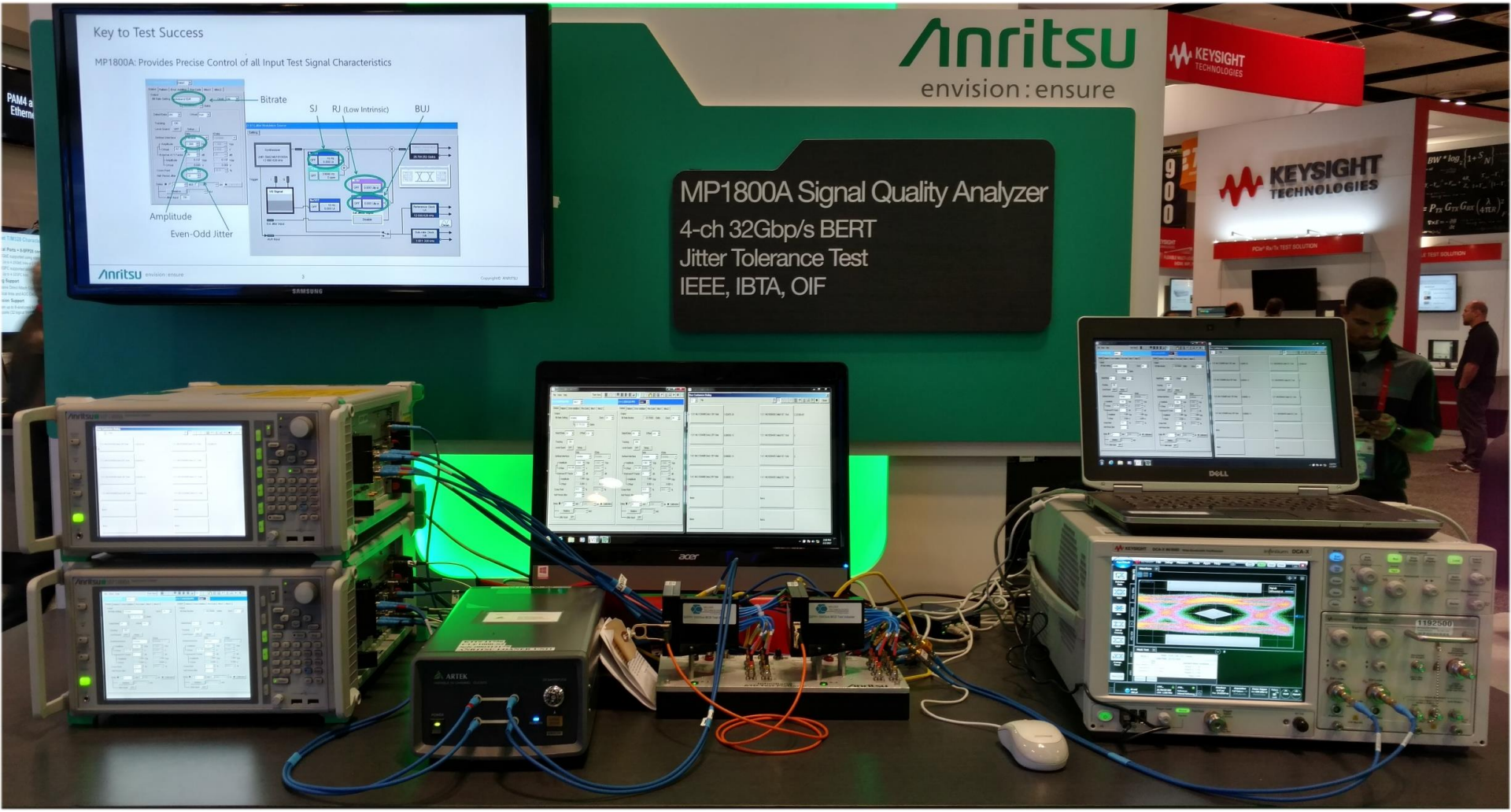
Cable Control *EEPROM Command Center*

- Developed by ***Software Forge*** for AOC management.
- Visual interface shows control and alarm activity.
- DUT features such as CTLE and CDR must be exercised to maximize chances of correct bit decisions.
- TX Clock & Data recovery at DUT Tx input reduces impact of jitter stresses applied by MP1800A Pattern Generators (likely to impact BER)
- Hardware CTLE compensates for frequency response of ISI channel, maximizing the chances of making correct bit decision. (likely to impact BER)
- Rx Clock & Data recovery further reduces waveform at far side of cable. (less likely to impact BER)



Adjust controls at cable input to optimize BER
Adjust controls at cable output to optimize signal quality.

IBTA EDR ATD System Implementation



Visit Anritsu Booth 633 for Live Demonstration

Path to InfiniBand HDR *(200G PAM4)*

Considerations for ATD / Stressed Receiver Testing:

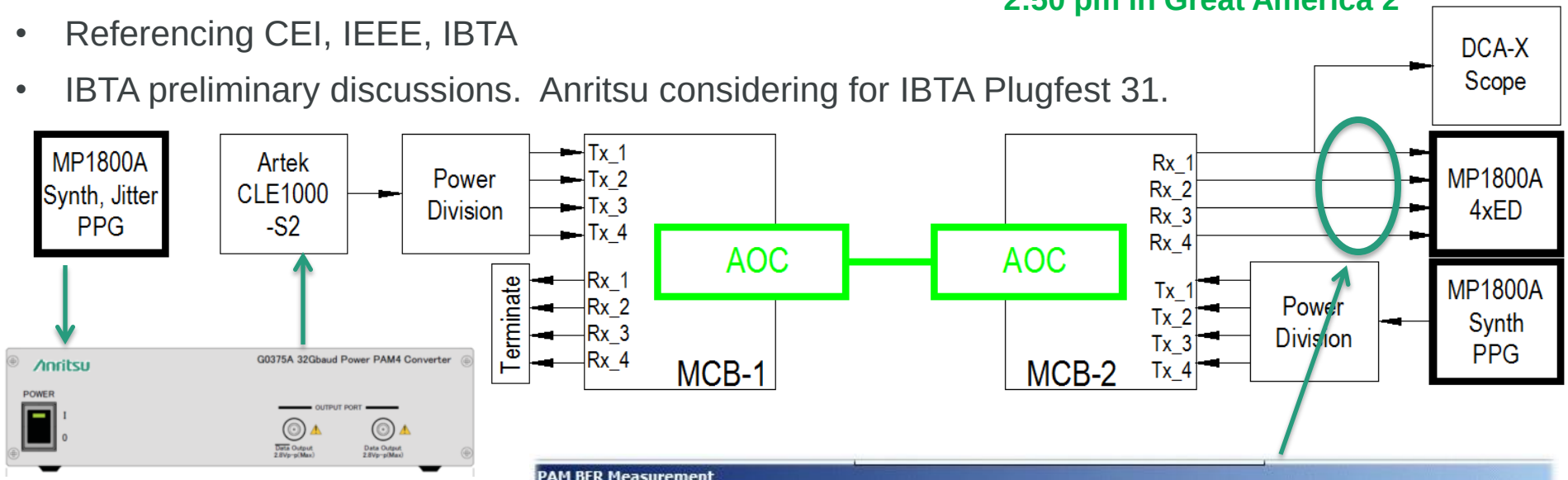
- Signal Generation / requirements / patterns used.
- BER Measurements
- Referencing CEI, IEEE, IBTA
- IBTA preliminary discussions. Anritsu considering for IBTA Plugfest 31.

Please attend Anritsu Session for more info

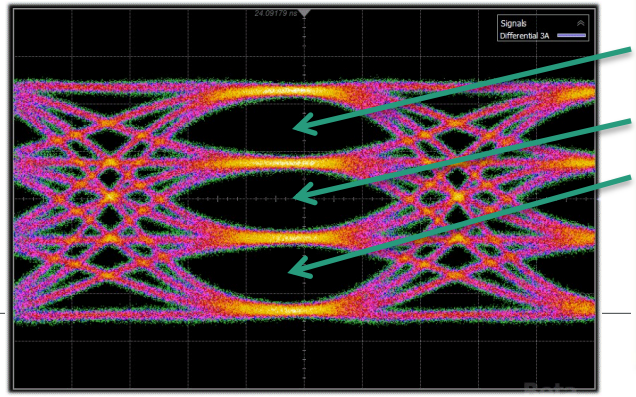
Toward 400G (IEEE802.3 and CEI)

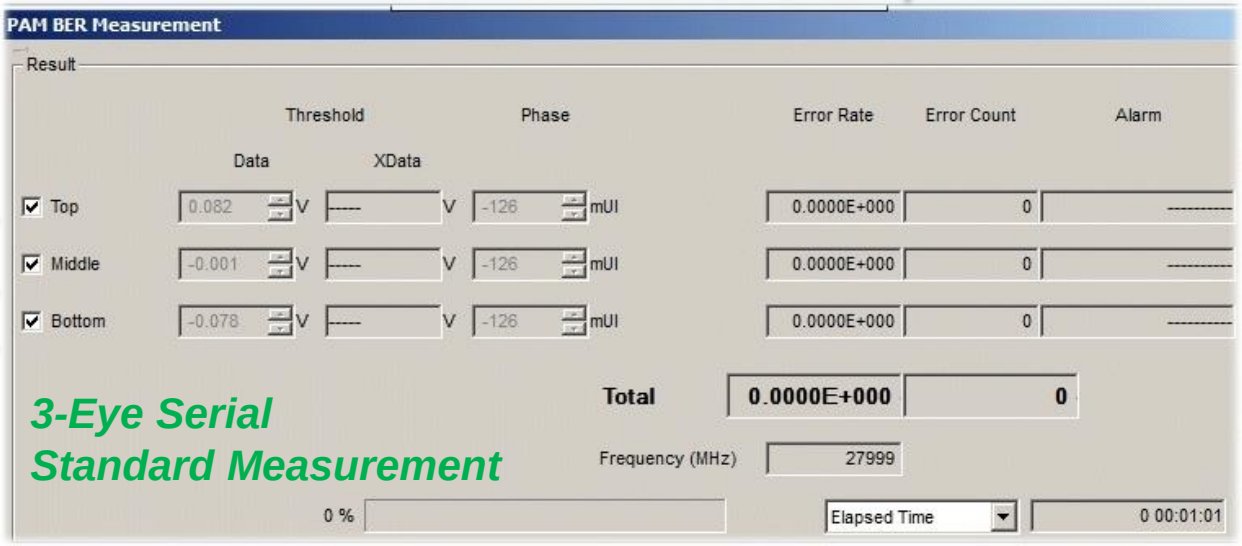
56G PAM4 Bit Error Rate Test Solution

2:50 pm in Great America 2



G0375A Power PAM4 Converter
4Vp-p Differential
See in Anritsu Booth #633





3-Eye Serial
Standard Measurement

Path to InfiniBand HDR *(200G PAM4)*

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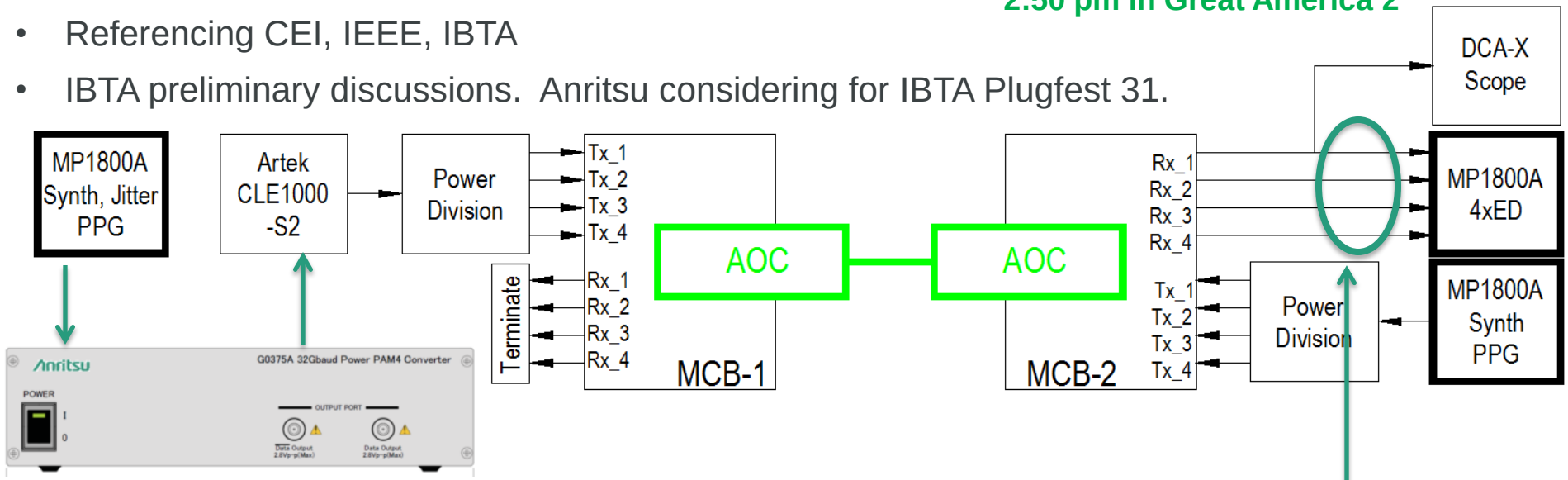
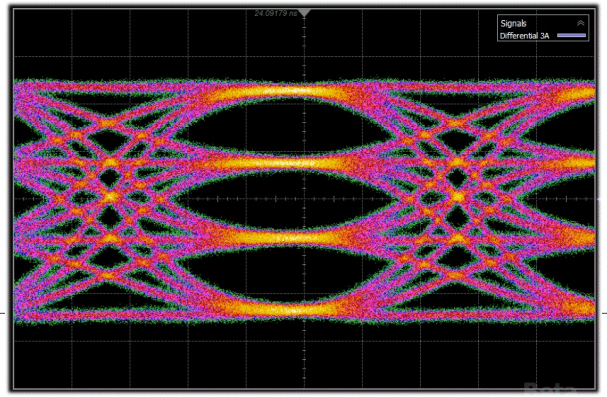
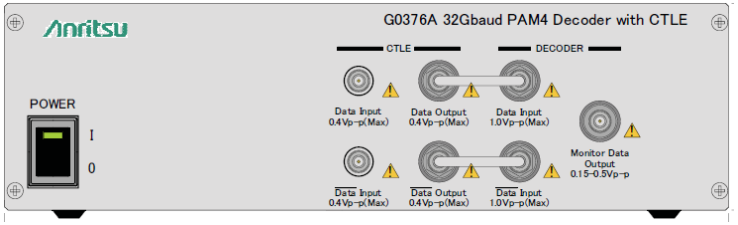
Toward 400G (IEEE802.3 and CEI)
56G PAM4 Bit Error Rate Test Solution
2:50 pm in Great America 2



G0375A Power PAM4 Converter
4Vp-p Differential
See in Anritsu Booth #633





G0376A PAM4 Decoder
See in Anritsu Booth #633

Wrap-Up

- For Cable/Module testing, much of the time & effort goes toward achieving a spec-compliant and calibrated test station.
- Accurate & repeatable calibration means trustworthy results.
- It is important for test equipment to provide reliable control and measurement of key signal parameters.
- High-performance / quality signals and components are required so external impairments do not influence DUT results.
- The solutions presented here satisfies these requirements with proven and robust test platforms that meet the industry's growing needs.

Thank You.

Visit Anritsu Booth 633 for Live Demonstration

Questions?

Anritsu

envision : ensure