InfiniBand Trade Association

Anritsu

Method Of Implementation

Active Time Domain Testing For FDR Active Cables

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Acknowledgements

This document would not have been possible were it not for contributions made by so many members of the InfiniBand Compliance & Interoperability Working Group and Electromechanical Working Group. Their generous inputs and tireless efforts were instrumental during Plugfest events and the development of this document.

Overview

This Method Of Implementation (MOI) contains information and procedures relevant to the Active Time Domain (ATD) testing performed at Plugfest events during which designers of Active Cables participate in interoperability testing of their products. Step-by-step procedures are provided throughout sections of this document which will guide the user through setup, calibrations and measurements designed to support interoperability testing of Active Cables with respect to the ATD parameters as defined in InfiniBand Architecture Specifications.

Glossary

This section provides definitions of the terminology used throughout this document. The reference diagram in Figure 1 is a considerably simplified representation of the ATD test system presented in this document, illustrating the terms defined in the glossary.

AOC	Active-Optical Cable assembly. Cable assemblies that use fiber–optic transceivers and fiber-optic interconnects to transmit high-speed serial data such as InfiniBand and Ethernet.
ATD	Active Time-Domain testing. A test methodology for active-cable-assemblies, (primarily Active Cable) where time-domain parameters such as jitter, eye-height and eye-width are measured on a stressed victim signal.
Cross-Talk	The phenomena of a signal transmitted on one channel coupling energy onto an adjacent channel, causing an undesirable effect.
Co-Propagating Input Aggressors	Adjacent channels which generate crosstalk energy and are driven from the input side of the test system and propagate in the same direction as the victim channel.
Counter-Propagating Output Aggressors	Adjacent channels which are driven from the output side of the test system, propagating in the opposite direction as the victim channel, and imposing crosstalk energy onto the victim channel at the output side of the ATD test system.
Counter-Propagating Input Aggressors	Adjacent channels which are driven from the output side of the test system, propagating in the opposite direction as the victim channel, and imposing crosstalk energy onto the victim channel at the input side of the ATD test system.
FEXT	Far-End Cross-Talk. Cross-Talk which occurs at the Far-End of a link. In ATD testing, the location of the Far-End is defined with respect to where the victim measurement is performed. FEXT will normally occur at the input of the ATD test system.
HCB	Host Compliance Board. PCB board or interface with known signal integrity characteristics that allow testing of host or switch specifications. The HCB is used for calibrating signals in the ATD test system. (HCB not illustrated below)
MCB	Module Compliance board. PCB board or interface with known signal integrity characteristics which allows testing of “modules” such as QSFP cable assemblies.
NEXT	Near-End Cross-Talk. Cross-Talk which occurs at the Near-End of a link. In ATD testing, the location of the Near-End is defined with respect to where the victim measurement is performed. NEXT will normally occur at the output of the ATD test system.
PPG	Pulse Pattern Generator. Signal generator used to generate pseudo random binary data for traffic.

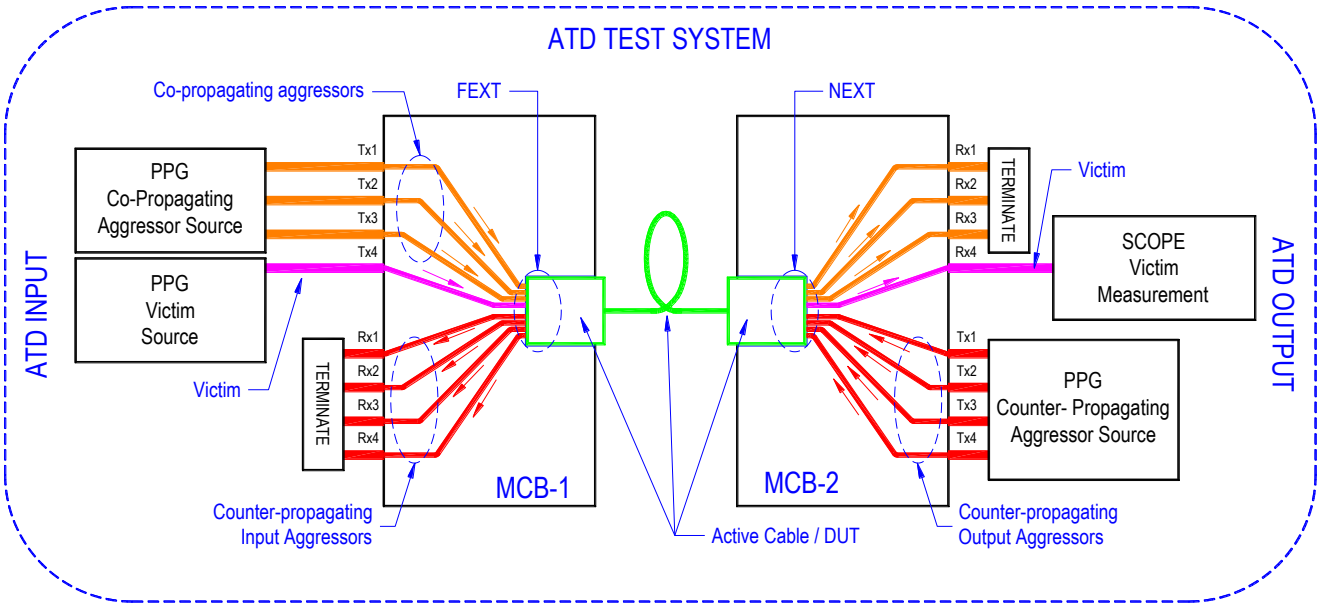

Figure 1. Glossary Reference Diagram

References

It is highly recommended that the following documents be read and understood prior to conducting the procedures and measurements described in this MOI.

- IBTA Volume 2 Physical Specification Draft - Latest Revision
- Anritsu – IB_FDR_AOC_appnote_E_0_00 - MP1800A Series – Active Optical Cable Evaluation Method

Equipment List

Item #	Description	Vendor	Part #	Qty	Function
1	MP1800A Mainframe A	Anritsu	MP1800A (*1)	1	Signal source for Victim and Co-Propagating Agressors.
2	MP1800A Mainframe B	Anritsu	MP1800A (*1)	1	Signal source for Counter-Propagating Agressors.
3	Emphasis	Anritsu	MP1825B (*1)	1	Equalization for Victim
4	Sampling Scope	Tektronix	DSA8300 (*2)	1	All time domain measurements.
5	Splitter_A	Anritsu	K240A (*3)	4	PPG signal division for driving all AOC lanes.
6	Splitter_B	Anritsu	K241A (*3)	8	PPG signal division for driving all AOC lanes.
7	MCB	Molex	1111143022	2	Module Compliance Board for AOC testing.
8	HCB	Wilder Technologies	QSFP+-TPA-HCB-P	1	Host Compliance Board (module) used for ATD calibration.
9	K Cables	Huber + Suhner	Sucoflex 104PE (*4)	21	Interconnect cables for driving AOC lanes & Sampling Scope
10	SMA Cables	-	*5	10	Interconnect cables for MP1800A Clocking and Scope Triggering
11	USB to I2C Adaptor	Mellanox	MTUSB-1	1	AOC Range Programming
12	I2C Interface Cable	-	*6	1	Interfaces between DB9 and MCB terminal block for programming
13	Power Supplies	CUI	EPAS-101W-05	2	AOC Power Supplies
14	PC	-	-	1	AOC Range Programming
15	Termination	-	-	14	Terminate unused ports during test and calibration

Table 1. Equipment List

Notes:

*1 Detailed Anritsu Equipment configurations provided in Table 3.

*2 Detailed Tektronix Equipment configurations provided in Table 2.

*3 Substitute part numbers may be used if BW / performance meets or exceeds that of part number indicated.

*4 Recommended BW > 26GHz and phase matched to ± 2ps.

*5 Recommended BW > 18GHz and phase matching not required. Length as required.

*6 See Appendix 1: FDR Range Programming .

Test Equipment Configuration

Plugfest events use the test equipment configurations shown in Table 2 and Table 3 during interoperability testing. These equipment options are provided for reference purposes and are not intended to suggest or represent the configuration for a comprehensive final production test solution.

Part Number	Options
DSA8300	Equivalent Time Digital Signal Analyzer
80E10B	50GHz Sampling Head
82A04B	30GHz Phase Reference

Table 2. Tektronix Equipment Configuration

Mainframe	Slot #	Part Number	Options
N/A	N/A	MP1825B	4 Tap Emphasis
		MP1825B-001	14 Gbit/s Operation
		MP1825B-003	14 Gbit/s Variable Data Delay
		MP1825B-005	14.1 Gbit/s Extension
-	-	MP1800A	SIGNAL QUALITY ANALYZER
		MP1800A-001	GPIB
		MP1800A-002	LAN
		MP1800A-014	2-Slot for PPG and/or ED
A	1, 2	MU181500B	Jitter Modulation Source
A	3	MU181020B	14 Gbit/s PPG
		MU181020B-002	0.1 to 14 Gbit/s
		MU181020B-005	14.1 Gbit/s Extension
		MU181020B-013	Variable Data Output (0.5 to 3.5 Vp-p)
		MU181020B-030	Variable Data Delay
A	4	MU181020B	14 Gbit/s PPG
		MU181020B-002	0.1 to 14 Gbit/s
		MU181020B-005	14.1 Gbit/s Extension
		MU181020B-013	Variable Data Output (0.5 to 3.5 Vp-p)
		MU181020B-030	Variable Data Delay
A	5, 6	MU181000A	12.5 GHz Synthesizer
B	-	MP1800A	SIGNAL QUALITY ANALYZER
		MP1800A-001	GPIB
		MP1800A-002	LAN
		MP1800A-014	2-Slot for PPG and/or ED
B	1, 2 **(*)**	MU181500B	Jitter Modulation Source
B	3	Not Used	Not Used
B	4	MU181020B	14 Gbit/s PPG
		MU181020B-002	0.1 to 14 Gbit/s
		MU181020B-013	Variable Data Output (0.5 to 3.5 Vp-p)
		MU181020B-030	Variable Data Delay
B	5, 6 **(*)**	MU181000A	12.5 GHz Synthesizer

Table 3. Anritsu Equipment Configuration

***** The Jitter Modulation Source in Mainframe B will NOT be used to apply jitter during this procedure. Its only purpose is to generate the 14GHz clock required for the proper operation of Mainframe B. The Jitter Modulation Source functionality includes an internal clock multiplier which will accept a 7GHz clock from the Synthesizer and produce a 14GHz clock for the pattern generator. This is necessary due to the Synthesizer's upper frequency limit of 12.5GHz. The above configuration was chosen for Plugfest events as a matter of convenience.

An acceptable alternate configuration would replace the MU181500B and MU181000A with an external synthesizer such as **Anritsu's MG3296C Signal Generator**. This unit can provide a direct 14GHz clock for the pattern generator in Mainframe B.

Overview of Fixture Calibration and DUT Testing

The setup and procedures described in this document utilize lane Tx4 sourced at the ATD input as the victim channel. Due to time constraints, this simplified test approach has been deemed adequate for the Active Cable auditing conducted at IBTA Plugfest events. It is by no means intended to represent a comprehensive Active Cable production test where each lane would be subjected to crosstalk and individually tested against compliance specifications.

A high-level overview of the steps involved in ATD Test Set calibration and DUT measurements are presented below. Each step will be described in greater detail in the pages that follow.

ATD Calibration:

1. Configure Anritsu systems per the procedures outlined in this document, referring to relevant application notes and standards when necessary.
2. Configure Tektronix measurement equipment per the procedures outlined in this document, referring to relevant application notes and standards when necessary. Ensure that applicable compliance masks are properly loaded into the measurement equipment.
3. Configure the power dividers and cables used to generate aggressor traffic.
4. Perform Calibration Step 1: FEXT Counter-Propagating Aggressors
5. Perform Calibration Step 2: FEXT Co-Propagating Aggressors
6. Perform Calibration Step 3: Victim Input Signal Calibration
7. Make any final adjustments needed to FEXT Co-Propagating Aggressors
8. Perform Calibration Step 4: NEXT Counter-Propagating Aggressors
9. Record all equipment settings at the conclusion of the calibration steps.

ATD Measurement:

1. Ensure that all calibration steps have been performed prior to conducting Active Cable measurements.
2. Configure equipment to perform Active Cable testing.
3. Apply victim signal and all aggressors to the MCB's
4. Configure the Active Cable for the proper amplitude range.
5. Perform ATD measurements.
6. Record data in approved spreadsheets or forms.

Anritsu Equipment Connections

The test equipment as shown in Figure 2 will source all data and clocking signals required to perform ATD testing. The highly configurable nature of the MP1800A test systems allows data and clock sources to be designated differently than what is depicted below. Figure 2 represents the test equipment configuration and connections implemented at Plugfest events. Ensure these equipment connections are in place before proceeding.

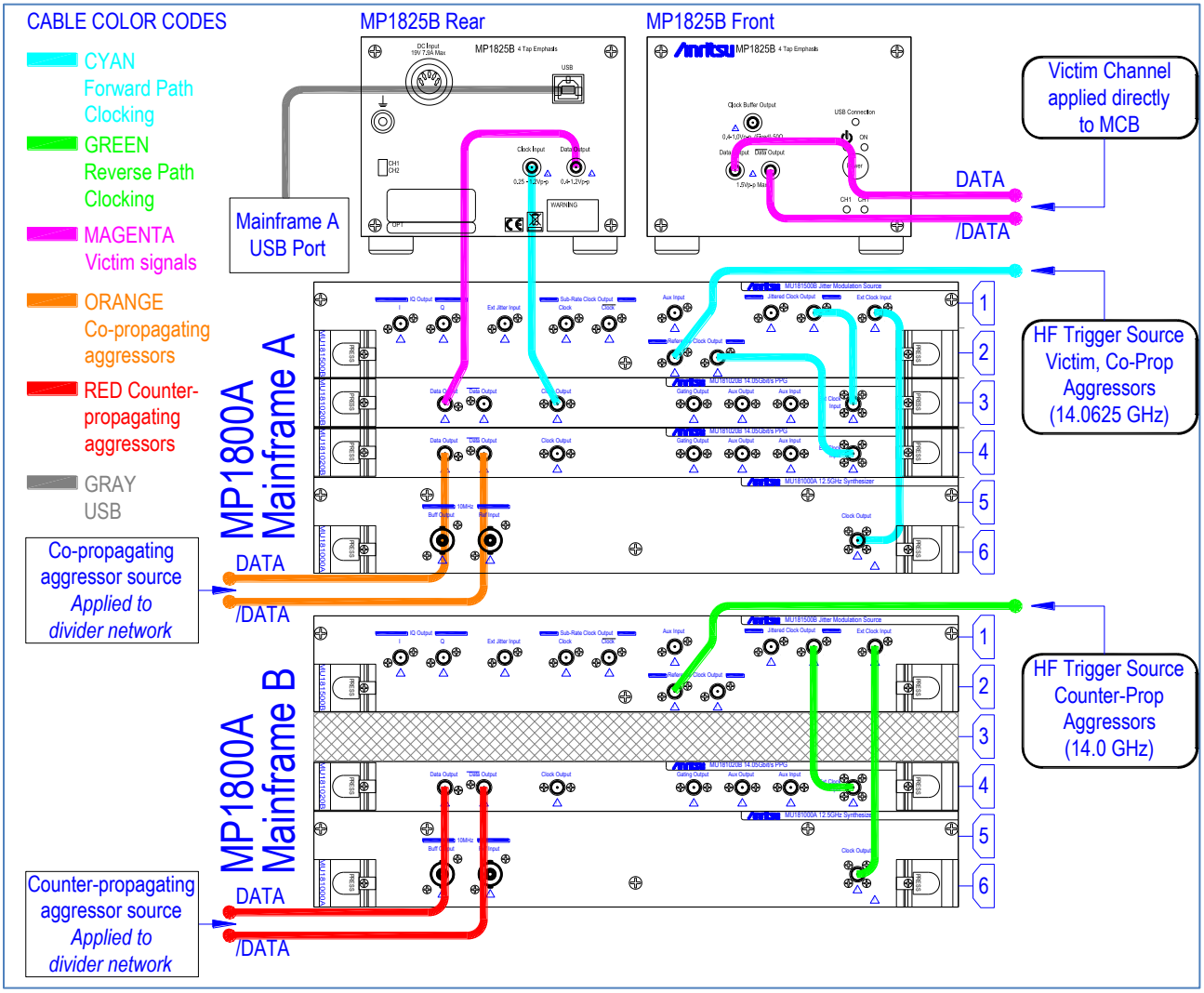

Figure 2. Equipment Configuration & Connections

Mainframe	Slot #	Part #	Type	Function
n/a	n/a	MP1825B	Emphasis	Signal equalization for the victim
A	1 & 2	MU181500B	Jitter Modulation	Jittered clock signals for victim channel Clean clock signals for co-prop aggressors HF trigger signal for forward propagating signals
A	3	MU181020B	PPG	Signal source for victim
A	4	MU181020B	PPG	Signal source for co-propagating aggressors
A	5 & 6	MU181000A	Synthesizer	Clock source for co-propagating signals
B	1 & 2	MU181500B	Jitter Modulation	Clean clock signal for counter-propagating aggressors HF trigger signal for counter propagating signals
B	3	-	-	Not used
B	4	MU181020B	PPG	Signal source for counter-propagating aggressors
B	5 & 6	MU181000A	Synthesizer	Clock source for counter-propagating signals

Table 4. Equipment Functionality

Generating Aggressor Channels

Given the simplified nature of this test approach, aggressor traffic will be generated using passive power divider networks. The input to these networks will be differentially driven by the PPG outputs in order to generate differential aggressor traffic. It is important that power dividers be of high quality with consistent amplitude and phase matching characteristics between their input and output ports. Furthermore, to maintain amplitude and phase balance between complimentary signals and channels, it is recommended to use phase-matched cables when making connections between the divider outputs and their final connection points. The illustrations shown in Figure 3 describe the power divider configurations used for Plugfest events.

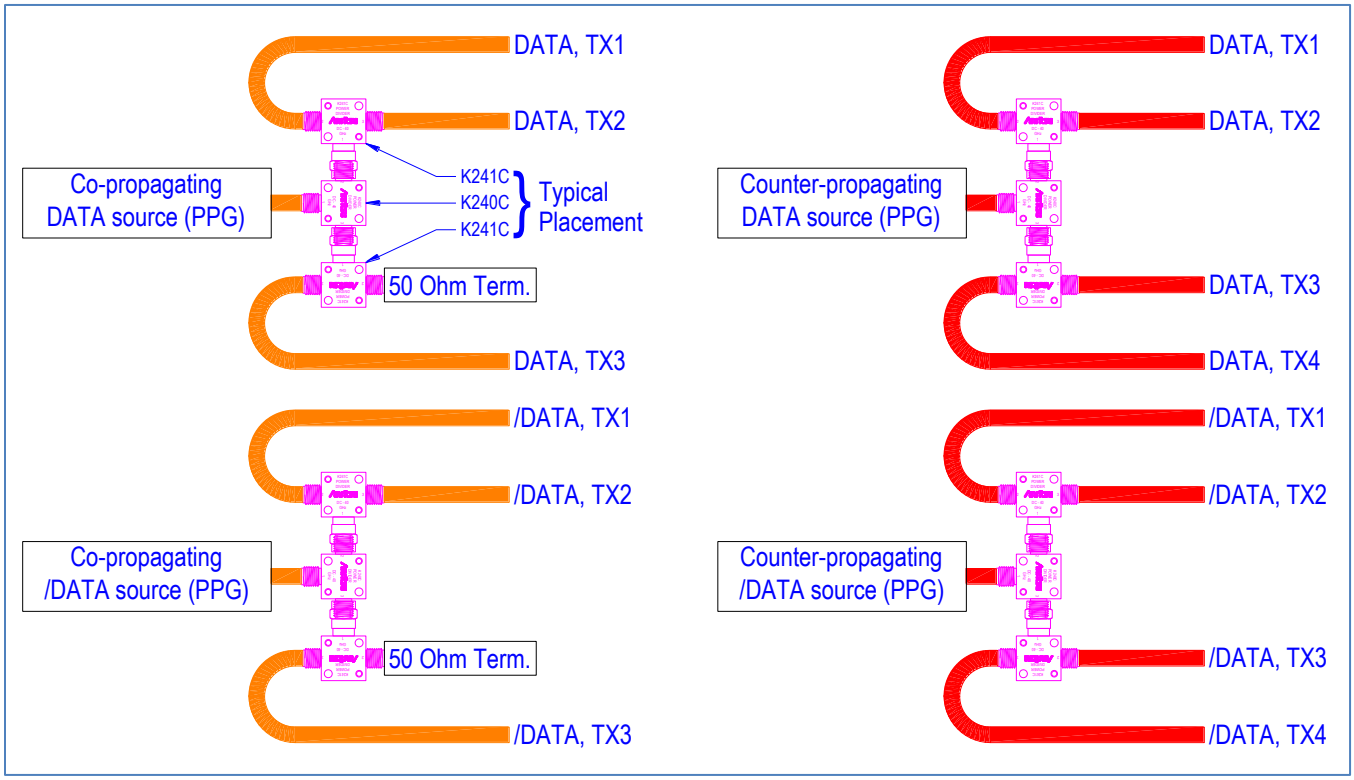

Figure 3. Power Divider Configurations

DATA and /DATA from the Co-propagating aggressor data source (Mainframe A / Slot 3) will each drive their own divider network, producing complimentary forward traffic for channels TX1, TX2 and TX3. Since channel TX4 (the victim) will be driven independently, the unused divider output must be terminated with 50Ω.

DATA and /DATA from the Counter-propagating aggressor data source (Mainframe B / Slot 3) will each drive their own divider network, producing complimentary reverse traffic for channels TX1, TX2, TX3 and TX4.

For simplification of future diagrams, all aggressor traffic including their PPG sources and respective divider networks will be represented using the images depicted in Figure 4. Each TX channel shown below represents a differential pair connection using phase matched cables.

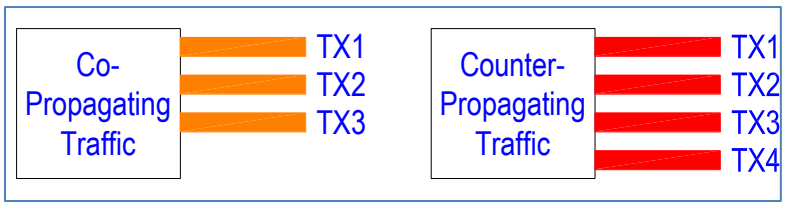

Figure 4. Aggressor Traffic Depiction

Differential Channel Observations

For the purpose of diagram simplification, signals within a differential pair will not be individually referenced. For example, the differential pair of TX1, DATA and TX1, /DATA will simply be referred to as TX1. The reader should assume that all traffic connections represented in this document are **differential**, and should be treated as such. This applies to signal sourcing as well as measurements and terminations. The following should be noted.

- It is important to always use phase matched cables at the input of measurement instruments to avoid adding unwanted delay between signals of a differential pair.
- When terminating channels, always terminate both signals of a differential pair with 50Ω. Failure to do so will result in an unbalanced load and an undesirable operating condition.
- Single-ended signaling will only be used for scope triggering.

Scope Measurements

The scope specified in the equipment list will be used for collecting all ATD data. Most of these measurements will be based on eye patterns. Table 5 defines various measurements that will be collected throughout the calibration and test steps outlined in this procedure.

Eye Diagram	A pattern created by an oscilloscope and sourced by a pseudorandom digital signal. This voltage level of this signal is sampled repeatedly while a synchronous clock signal triggers the scope's horizontal sweep. The eye pattern itself represents the superposition of all possible bit sequences in the pattern viewed within a single time interval. Eye patterns are typically used to comprehensively evaluate the effects of noise and inter-symbol interference on data signals.
Eye Mask	An eye mask is a tool that defines the allowable shape of an eye diagram. The mask test is defined by points in both the amplitude and time domains. ***All masks required to support the testing described in this document should be loaded into the scope before executing this procedure. Masks may be downloaded from:*** https://danahertm.box.com/s/e63icjum1eg2qhpgdt0u
Mask Hit Ratio	The ratio between the number of mask violations to the number of samples collected. For example 50 violations in 1,000,000 samples results in a hit ratio of 5 x 10^{-5}.
Eye Vp-p	Peak-to-peak voltage of an eye diagram. The difference between the maximum voltage and minimum voltage with respect to the displayed waveform. This should not be confused with eye amplitude which is a measurement based on statistical analysis of the logical "one" and "zero" level.
Rise / Fall Time	The amount of time required for a pulse to transition between 2 different logic states. The measurements within this document use 20% to 80% reference levels to characterize transition speed.
J2 Jitter	The total jitter that would result in a bit error rate of 2.5 x 10^{-3}
J9 Jitter	The total jitter that would result in a bit error rate of 2.5 x 10^{-10}
DDWPS	Data Dependent Pulse Width Shrinkage. Expressed as a decrease in the pulse width caused by inadequate bandwidth and reflections in the transmission path.

Table 5. Scope Measurement Terminology

Active Cable Voltage Range Programming

The range settings for FDR Active Cables are stored in volatile section of the QSFP memory and must be re-set each time a cable is powered up for test. Range settings are accessed on Page 3 bytes 238 and 239 (0xEE and 0XFF). The Mellanox I2C to USB adaptor is used at Plugfest events to program the proper bytes as follows:

- The Active Cable QSFP connection to MCB-2 will be set to Range 0 by setting bytes 238 and 239 to "zero". This represents the lowest signal range resulting in the highest susceptibility to NEXT for the victim.
- The Active Cable QSFP connection to MCB-1 will also be set to Range 0 by setting bytes 238 and 239 to "zero".
- See Appendix 1 for instructions on programming the Active Cable range settings.

Calibration Step 1: Counter-Propagating FEXT Aggressors

The goal of this calibration step is to set the amplitude of the counter-propagating aggressors at the input side of the ATD test system. This calibration step will ensure that proper counter-propagating aggressor crosstalk will be present when the victim calibration is performed in later steps. Counter-propagating aggressor signals will be applied via the HCB and measured at corresponding points on MCB-1 using the scope. Refer to Figure 5 while executing the following steps.

1. Connect the HCB to the MCB-1 to create a mated pair as shown.
2. Connect counter-propagating traffic to the corresponding RX connectors on the HCB.
3. Co-propagating and victim channels may be off at this time.
4. Properly terminate all TX channels on the HCB to 50Ω.
5. Make sure Scope is triggered by the HF trigger source for counter-propagating signals as defined in Figure 2.
6. Measure each of the counter-propagating channels (RX1, RX2, RX3, RX4) on MCB-1 at TP7a using the Scope, making sure that all RX channels not being measured have been properly terminated to 50Ω.
7. Adjust PPG amplitude settings for the counter-propagating aggressors so that eye Vp-p measurements for all RX channels at TP7a are set to the targets shown in Table 6.

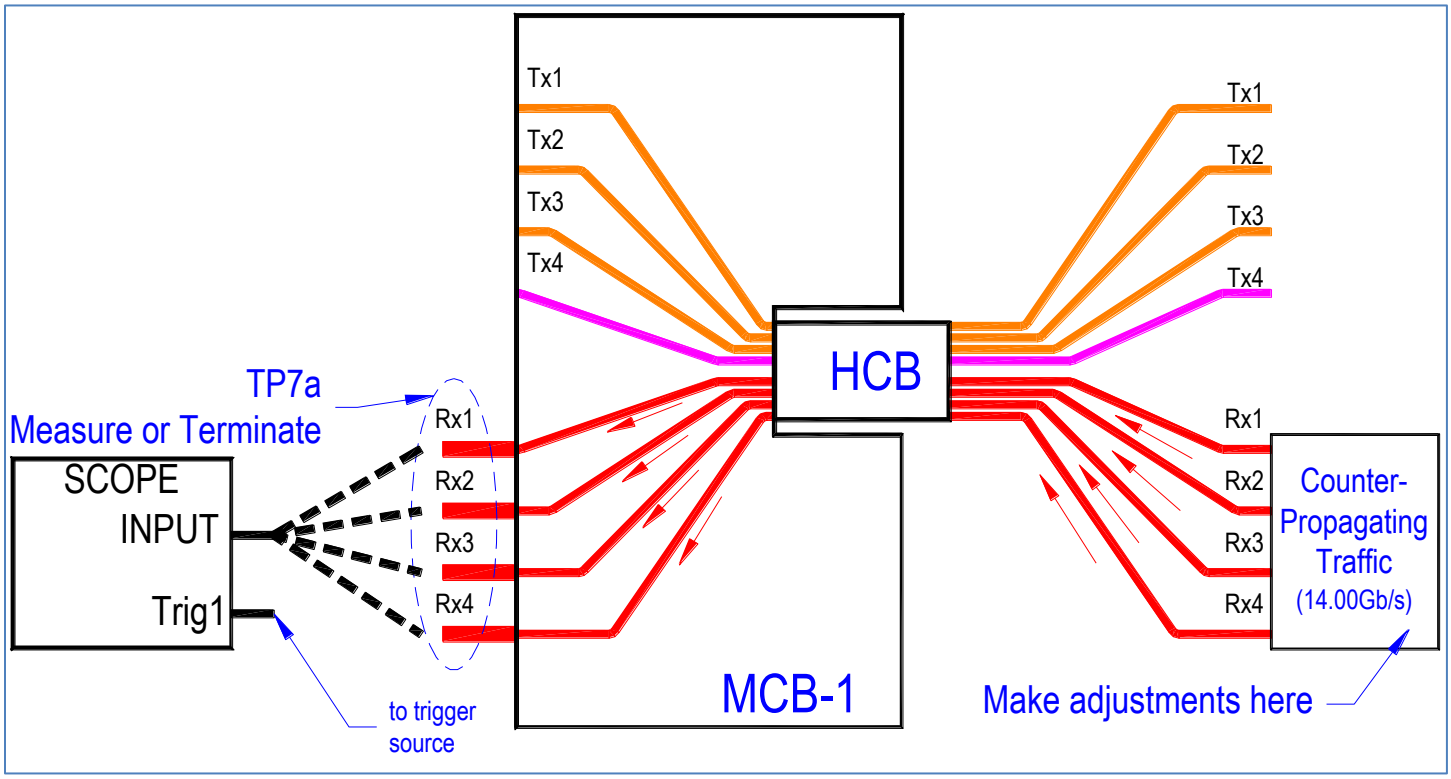

Figure 5. Counter-propagating FEXT aggressor calibration setup

Parameter	Target Value	Mainframe	Slot	Equipment Adjustment Menu
Data Rate	14.00 Gb/s	B	2	Synthesizer Frequency Setting
Pattern	PRBS 31	B	3	Pattern Tab >> Set PRBS 2^31-1
Max Eye Vp-p	450mV	B	3	Output Tab >> Adjust Amplitude value
Min Transition Time	17ps (20% - 80%)	-	-	*Not adjustable by equipment*

Table 6. Target counter-propagating FEXT aggressor specs and corresponding equipment controls

Calibration Step 2: Co-Propagating FEXT Aggressors

The goal of this calibration step is to set the INITIAL amplitude of the co-propagating aggressors at the input side of the ATD test system. This calibration step will ensure that proper co-propagating aggressor crosstalk will be present when the victim calibration is performed in later steps. Co-propagating aggressor signals will be applied via MCB-1 and measured at corresponding points on the HCB using the scope. Note that a FINAL check and possible adjustment of the co-propagating aggressors will be executed AFTER the victim calibration is performed. Refer to Figure 6 while executing the following steps.

1. Keep the HCB / MCB-1 mated pair created in the last calibration section.
2. Properly terminate all RX channels on MCB-1.
3. Verify that co-propagating traffic is connected to the corresponding TX connectors on the MCB-1.
4. Victim and counter-propagating channels may be off at this time.
5. Make sure Scope is triggered by the HF trigger source for victim / co-propagating signals as defined in Figure 2.
6. Measure each of the co-propagating channels (TX1, TX2, TX3) on the HCB at TP6a using the Scope, making sure that all TX channels not being measured have been properly terminated to 50Ω.
7. Adjust PPG amplitude settings for the co-propagating aggressors so that Eye Vp-p measurements for all TX channels at TP6a are set to the INITIAL target shown in Table 7.
8. **AFTER performing Calibration Step 3: Victim Input Signal Calibration (next page), return to this configuration and verify that Eye Vp-p for all co-propagating aggressors meets the FINAL target shown in Table 7.**

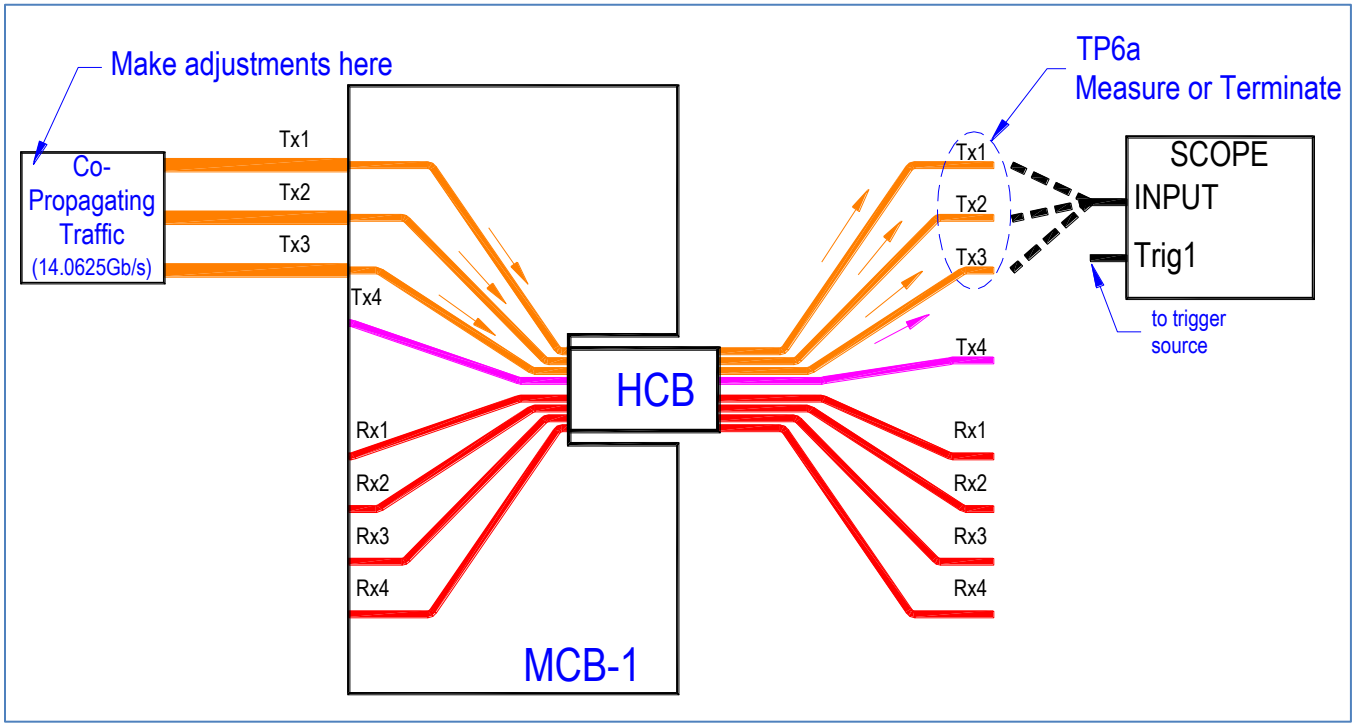

Figure 6. Co-Propagating FEXT aggressor calibration setup

Parameter	Target Value	Mainframe	Slot	Equipment Adjustment Menu
Data Rate	14.0625 Gb/s	A	2	Synthesizer Frequency Setting
Pattern	PRBS 31	A	4	Pattern Tab >> Set PRBS 2^31-1
Max Eye Vp-p (INITIAL)	450mV	A	4	Output Tab >> Set Amplitude value
Max Eye Vp-p (FINAL)	Victim Eye Vp-p ± 20%	A	4	Output Tab >> Adjust Amplitude value
Min Transition Time	17ps (20% - 80%)	-	-	*Not adjustable by equipment*

Table 7. Target Co-Propagating FEXT aggressor specs and corresponding equipment controls

Calibration Step 3: Victim Input Signal Calibration

The goal of this calibration step is the creation of a properly-stressed victim channel to be the source signal for the Active Cable DUT measurement. This channel will be calibrated in the presence of the recently calibrated aggressor traffic. During this calibration step, aggressor traffic will be applied in the same manner as described in previous steps while victim eye parameters are adjusted to achieve compliance to a calibration mask. Refer to Figure 7 while executing the following steps.

1. Keep the HCB / MCB-1 mated pair created in the last calibration section.
2. Properly terminate all RX channels on MCB-1 and TX1, TX2, TX3 on the HCB to 50Ω.
3. Connect all aggressor traffic to MCB-1 and the HCB at this time.
4. Make sure Scope is triggered by the HF trigger source for victim / co-propagating signals as defined in Figure 2.
5. Measure the victim channel parameters on TX4 of the HCB using the Scope.
6. Adjust victim settings to simultaneously achieve all the parameter targets shown in Figure 8, Table 8 and Table 9.
7. See **Appendix 2: Setting DDWPS, J2, J9, Eye Mask Parameters** for parameter setting procedures.
8. ***Victim Channel amplitude setting is ideal when specified hit ratio is achieved with ALL hits occurring in Eye Mask AREA 2.***
9. **After victim calibration, return to Calibration Step 2: FEXT Co-Propagating Aggressors to verify that Eye Vp-p for all co-propagating aggressors meet the FINAL target shown in Table 7.**

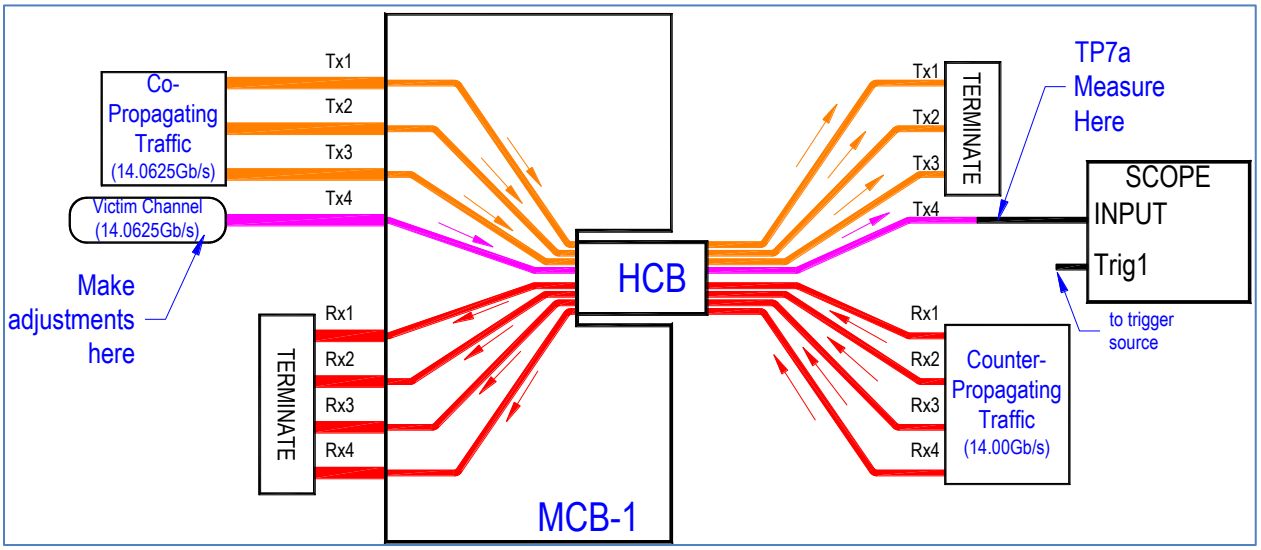

Figure 7. Victim calibration setup

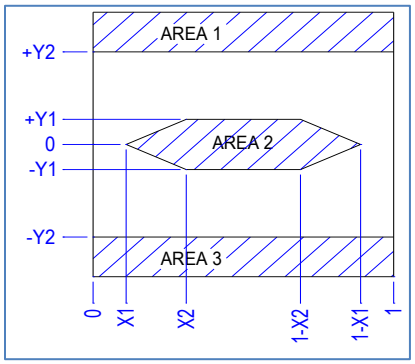

Figure 8. Victim Input Eye Mask

Mask Point	Spec Value
X1	0.11 UI
X2	0.31 UI
Y1	95 mV
Y2	350 mV

Table 8. Eye Mask Definition

Parameter	Target Value	Equipment Adjustment Notes
Data Rate	14.0625 Gb/s	Set using Mainframe A / Slot 2 (Jitter Modulation Source)
1 UI	71.111 ps	Synthesizer settings
Mask Hit Ratio PRBS 31	$< 5 \times 10^{-5}$	Adjust using MP1825B Amplitude and Tap control Achieve target hit ratio with hits ONLY in mask AREA 2 Target this limit during calibration
J2 PRBS 31	13.51 ps (0.19 UI)	Set using Mainframe A / Slot 2 (Jitter Modulation Source) Primary control for J2 is Sinusoidal Jitter (SJ) Turn SJ ON and adjust SJ Frequency to 100MHz Adjust jitter amplitude to achieve target J2 value
J9 PRBS 31	24.14 ps (0.34 UI)	Set using Mainframe A / Slot 2 (Jitter Modulation Source) Primary control for J9 is Random Jitter (RJ) Turn RJ ON and select NONE for filter Adjust jitter amplitude to achieve target J9 value
DDPWS PRBS 9	7.82 ps (0.11 UI)	Adjust using MP1825 tap control

Table 9. Target Victim specs and corresponding equipment controls

Calibration Step 4: Counter-Propagating NEXT Aggressors

The goal of this calibration step is to set the amplitude of the counter-propagating aggressors at the output side of the ATD test system that will correspond to Infiniband specifications. Counter-propagating aggressor signals will be applied via MCB-2 and measured at corresponding points on the HCB using the scope. Refer to Figure 9 while executing the following steps.

1. Connect the HCB to the MCB-2 to create a mated pair as shown.
2. Co-propagating and victim channels may be off at this time.
3. Connect counter-propagating aggressor traffic to MCB-2.
4. Make sure Scope is triggered by the HF trigger source for counter-propagating signals as defined in Figure 2.
5. Measure each of the counter-propagating channels (TX1, TX2, TX3, TX4) on the HCB using the Scope, making sure that any TX channels not being measured have been properly terminated to 50Ω.
6. Adjust PPG amplitude settings for the counter-propagating aggressors so that Eye Vp-p measurements for all TX channels are set to the target shown in Table 10.

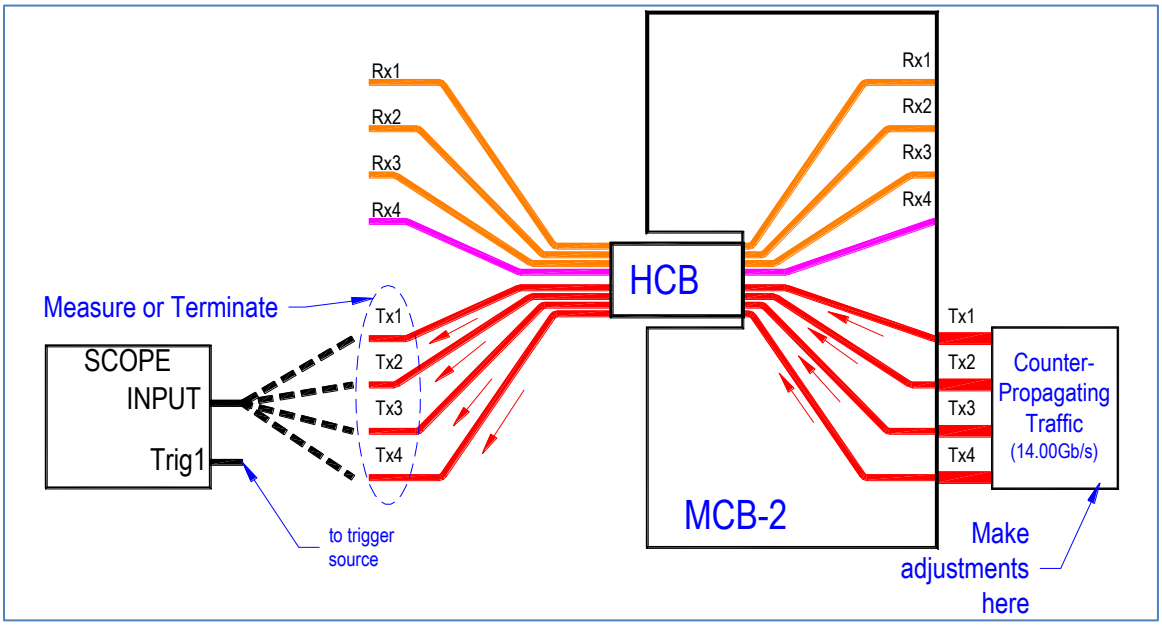

Figure 9. Counter-propagating NEXT aggressor calibration setup

Parameter	Target Value	Mainframe	Slot	Equipment Adjustment Menu
Data Rate	14.00 Gb/s	B	2	Synthesizer Frequency Setting
Pattern	PRBS 31	B	3	Pattern Tab >> Set PRBS 2^31-1
Max Eye Vp-p	700mV	B	3	Output Tab >> Adjust Amplitude value
Min Transition Time	17ps (20% - 80%)	xx	xx	*Not Adjustable by equipment*

Table 10. Target counter-propagating NEXT aggressor specs and corresponding equipment controls

DUT Testing

Only after completing the multi-step calibration process is the system ready for the ATD measurements described in this section. The goal of this section is to determine spec compliance of the victim channel (forward propagating channel TX4) in the presence of stress and aggressor traffic which was set up during the calibration process. Refer to Figure 10 while executing the following steps.

1. Connect all test equipment as shown, applying Victim and Aggressor traffic using equipment settings determined during the previous calibration steps.
2. Make sure Scope is triggered by the HF trigger source for victim signals as defined in Figure 2.
3. Connect the Active Cable DUT between MCB-1 and MCB-2, mating the specific cable end to the correct MCB as predetermined by the auditing / test requirements (if any).
4. Apply DC power to the MCB boards.
5. Attach the I2C interface cable to the MCBs to program their respective Active Cable ranges.
6. Program BOTH the MCB-1 cable end AND the MCB-2 cable end for **Range 0**.
7. Perform scope measurements as defined by the parameters in Figure 11, Table 11 and Table 12. See Appendix 5: Sample Victim Output Measurement.
8. Record all measured values in proper DUT spreadsheet or form.

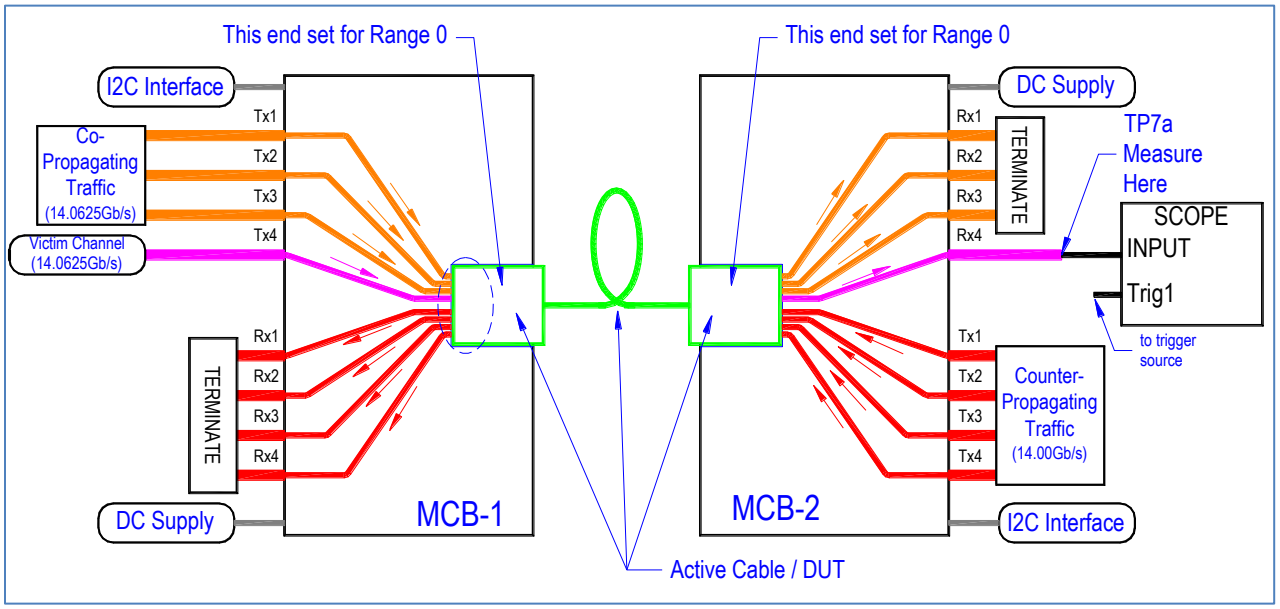

Figure 10. DUT Test Configuration

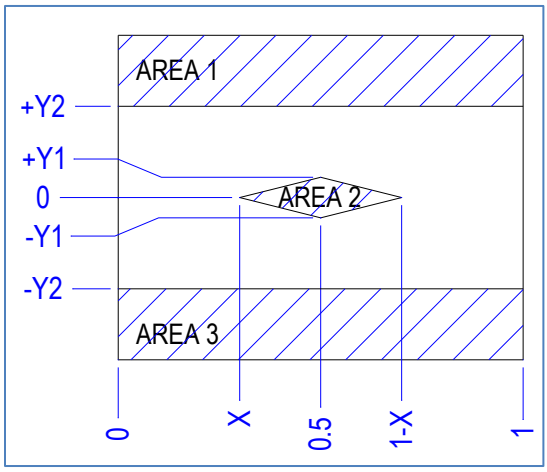

Figure 11. Victim Output Eye Mask

Mask Point	Spec Value
X	0.30 UI
Y1	50 mV
Y2	225 mV

Table 11. Eye Mask Definition

Parameter	Specification
Data Rate	14.0625Gb/s
Pattern	PRBS 31
Mask Hit Ratio (4k waveforms)	$< 5 \times 10^{-5}$
J2 (20M samples)	< 31.28 ps (0.44 UI)
J9 (20M samples)	< 49.06 ps (0.69 UI)

Table 12. Victim Output Specifications

Appendix 1: FDR Range Programming and Interface Cable Construction

The commands below were used to program the cables for the correct amplitude ranges using the PC designated for Plugfest events.

Setting Range 0

```
cd C:\Program Files (x86)\Diolan\I2CBridge.x64\bin
i2c r -s:0x50 -a:0x1:0x7f -d:0x1
i2c w -s:0x50 -a:0x1:0x7f -d:0x1 3
i2c r -s:0x50 -a:0x1:0x7f -d:0x1
i2c r -s:0x50 -a:0x1:0xee -d:0x1
i2c w -s:0x50 -a:0x1:0xee -d:0x1 00
PING 127.0.0.1 -n 1 >nul
i2c r -s:0x50 -a:0x1:0xef -d:0x1
i2c w -s:0x50 -a:0x1:0xef -d:0x1 00
PING 127.0.0.1 -n 1 >nul
i2c r -s:0x50 -a:0x1:0xee -d:0x2
```

I2C Interface Cable

The interface cable creates the data connection between the Mellanox USB to I2C Adapter and the MCB. The interface cable can be constructed by following these steps:

1. Use a standard DB9 Female serial cable approximately 1 – 2 feet in length.
2. Strip about 3 inches of the outer jacket from the free end.
3. Identify the following wires that will be used to interface to the MCB
   a. RED – SCL – (DB9 Pin 8)
   b. GREEN – SDA (DB9 Pin 6)
   c. WHITE – GND (DB9 Pins 1, 2, 3, 4, 5)
4. Strip about 0.5” from the ends of each of these wires.
5. Insert each wire into the corresponding connection of the MCB terminal block and tighten screws.
6. Final connections to MCB should resemble Figure 12

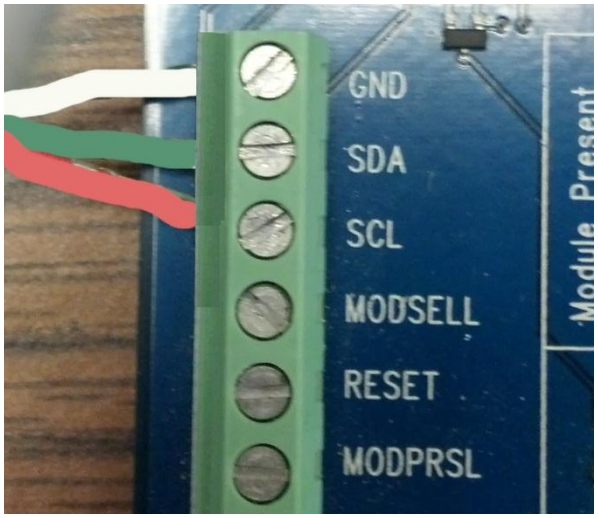

Figure 12. I2C Interface Cable

Appendix 2: Setting DDWPS, J2, J9, Eye Mask Parameters

Achieving simultaneous spec compliance for DDPWS, J2, J9 and the Eye Mask requires the adjustment of multiple test equipment settings. This section will guide the user through those adjustments. The instructions listed below reference points (x) indicated in the GUI screens of Figure 13 and Figure 14.

1. Turn MP1825B Output (A) and Emphasis Function (B) on.
2. Click the calibration button (C) if its indicator is red.
3. Set Cursors 1, 2, 3 (D, E, F) to 0.0 dB. Note that during this procedure only Cursor 1 will be adjusted.
4. Set initial eye amplitude (G) to achieve compliance to the victim input eye mask as defined in Figure 8, Table 8 and Table 9. Final adjustments of this parameter will be made at the conclusion of tuning.
5. Adjust Cursor 1 (D) to achieve DDPWS as defined by the conditions and limits of Table 9.
    a. Decrease value of Cursor 1 to increase DDPWS. Increase value of Cursor 1 to decrease DDPWS.
6. Set Sinusoidal Jitter (J) frequency to 100MHz and turn on.
7. Turn Random Jitter (K) on. Make sure filters are disabled while adjusting this parameter.
8. Adjust SJ (J) value to achieve J2 as defined by the conditions and limits of Table 9.
    a. Decrease value of SJ to decrease J2. Increase value of SJ to increase J2.
9. Adjust RJ (K) value to achieve J9 as defined by the conditions and limits of Table 9.
    a. Decrease value of RJ to decrease J9. Increase value of RJ to increase J9.
10. Note that J2, J9 and DDPWS compliance must be achieved simultaneously as defined by the conditions and limits of Table 9. ***Some fine-tuning of equipment settings will be required to achieve simultaneous compliance.***
11. Once J2, J9 and DDWPS compliance has been achieved, make final adjustments to eye amplitude (G) so that eye mask hit ratio is achieved. Target the upper limit as defined by the conditions and limits of Table 9, **with ALL HITS occurring in Mask AREA 2.**

12. Record all equipment settings at the conclusion of this tuning process.

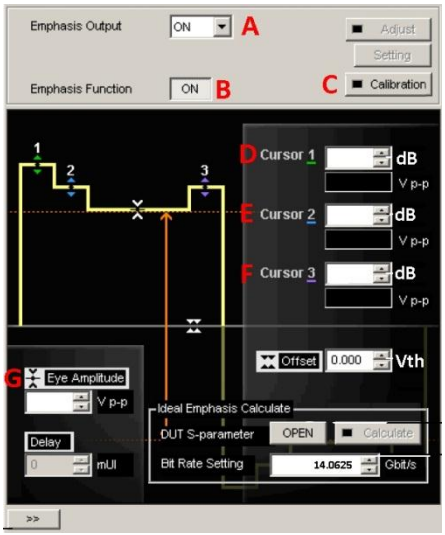

Figure 13. MP1825B Control Screen

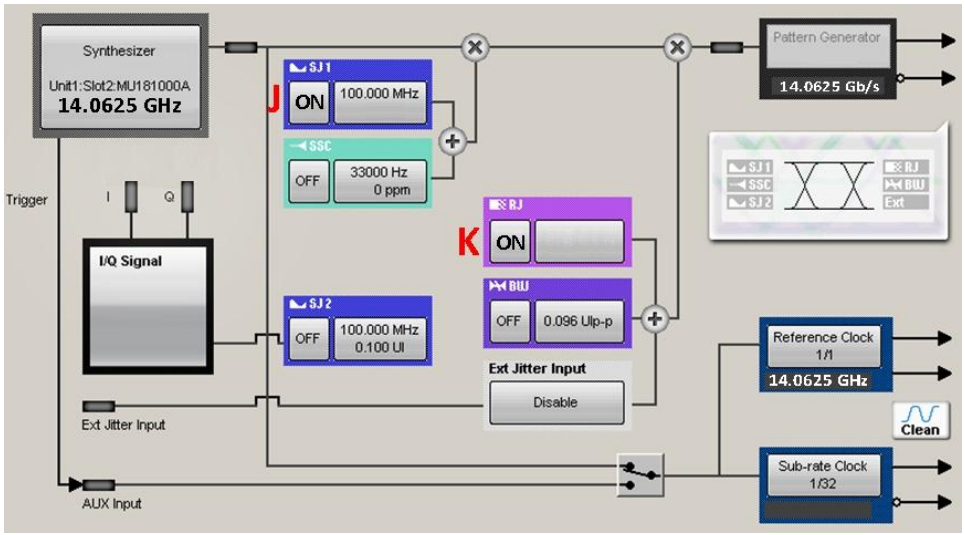

Figure 14. MU181500B (Mainframe A) Control Screen

Appendix 3: Plugfest 24 FDR Equipment Settings

The table below contains the Anritsu equipment settings as determined by the FDR calibration process.

Mainframe	Module	Slot	Function	Equipment Setting
USB to Mainframe A	MP1825B	External	Emphasis & Amplitude Victim Channel	Bit rate = 14.0625Gb/s AC Coupled ON Single-Ended Amplitude = 200mV (Differential Amplitude = 400mV) Cursor 1 = -1.0dB, Cursor 2 = 0dB, Cursor 3 = 0dB
A	MU181500B	1, 2	Jitter Module	Bit rate = 14.0625Gb/s SJ = 0.090UI @ 100MHz, RJ = 0.324UI
A	MU181020B	3	Pulse Pattern Generator Victim Channel	Bit rate = 14.0625Gb/s Amplitude controlled by MP1825B Pattern adjusted per test specification
A	MU181020B	4	Pulse Pattern Generator Co-prop aggressors	Bit rate = 14.0625Gb/s, Pattern = PRBS31 AC Coupled ON, Data, /Data amplitude tracking ON Cal Amplitude = 1.0V
A	MU181000A	5, 6	Synthesizer	Frequency controlled by Jitter Module
B	MU181500B	1, 2	Jitter Module	Bit rate = 14.0Gb/s No Applied Jitter
B	-	3	NOT USED	NOT USED
B	MU181020B	4	Pulse Pattern Generator Counter-prop aggressors	Bit rate = 14.0Gb/s, Pattern = PRBS31 AC Coupled ON, Data, /Data amplitude tracking ON FEXT Cal Amplitude = 0.740V NEXT Cal Amplitude = 1.100V
B	MU181000A	5, 6	Synthesizer	Frequency controlled by Jitter Module

Table 13. Anritsu Equipment Settings

Appendix 4: Setup Photographs

Figure 15. ATD Test Station

Figure 16. MCBs and Interconnections

Appendix 5: Sample Victim Output Measurement

The sample data screen shows a captured FDR waveform with all relevant scope parameters shown on the screens.

- Passing J2 / J9 data.
- No mask violations in any of the mask regions following the acquisition of 4k waveforms

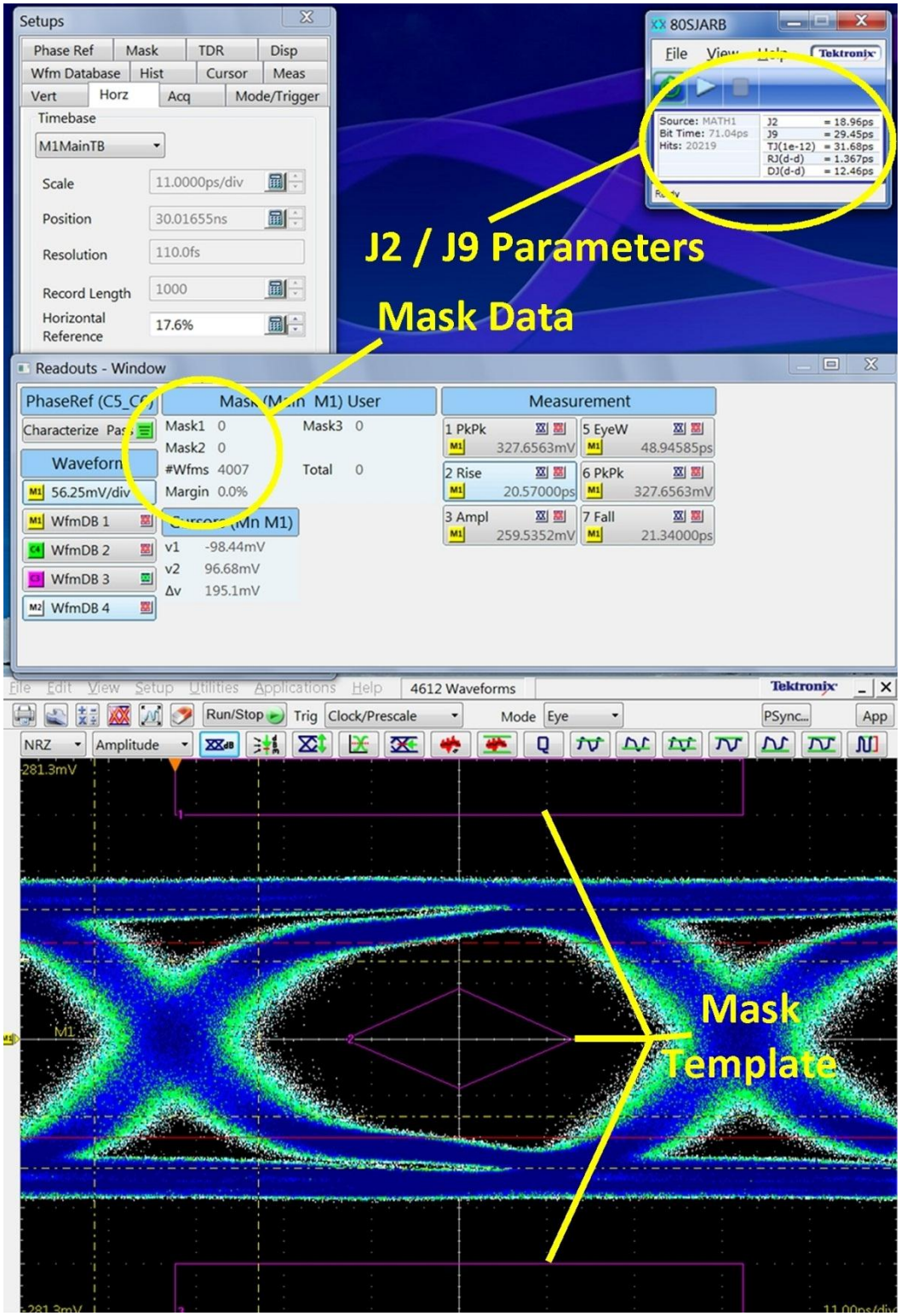

Figure 17. Sample Victim Output Measurement

Appendix 6: Relevant InfiniBand Specification Tables

The following tables are excerpts from InfiniBand Architecture Specification Volume 2, Release 1.2.1

Figure 199, Table 84, Table 85 are references within the Specification.

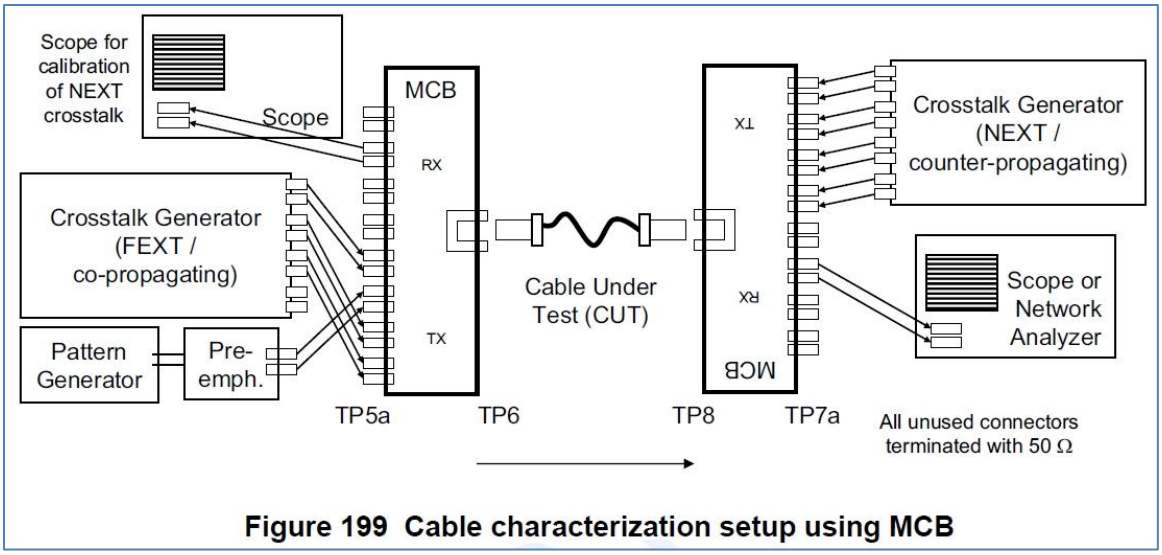

Figure 18. InfiniBand Spec ATD Diagram

Table 84 FDR limiting active cable input electrical specifications

Symbol	Parameter	Specification value(s)	Unit	Conditions
X1, X2	eye mask parameter, time; see Figure 87 on page 276	0.11, 0.31	UI	At TP6a, at FDR and higher data rates Hit ratio=$5x10^{-5}$
Y1, Y2	eye mask parameter, voltage	95, 350	mV	
	Crosstalk signal Vpk-pk	+/- 20% (See Conditions)	mV	At TP6a. Co-propagating aggressors. Crosstalk signal Vpk-pk to match lane under test, to within +/- 20%.
	Crosstalk signal transition time, 20%-80%	24	ps	
	Crosstalk calibration signal Vpk-pk, each aggressor	450	mV	At TP7a. Counter-propagating aggressors. Apply during crosstalk calibration only[a]
	Crosstalk calibration signal transition time, 20%-80%	17	ps	

Symbol	Parameter	Max	Min	Unit	Conditions
	Single-ended input voltage	4	-0.3	V	At TP6a
V_{CM}	AC common mode input voltage tolerance (RMS)	20		mV	At TP6a
DDPWS	Data Dependent Pulse Width Shrinkage	0.11		UI	At TP6a
J2	J2 Jitter tolerance	0.19		UI	At TP6a
J9	J9 Jitter tolerance	0.34		UI	At TP6a
S_{DD11}	Differential input return loss	Eq. 1 on page 287		dB	At TP5a, 50 MHz to 14.1 GHz
S_{CC11}	Common mode input return loss	-2		dB	At TP5a, 200 MHz to 14.1 GHz
S_{DC11}	Common mode to differential reflection	Eq. 2 on page 287		dB	At TP5a, 50 MHz to 14.1 GHz

a. Please refer to CIWG Method of Implementation (MOI) document Active Time Domain Testing for detailed specification of testing methodology and parameters.

Figure 19. Infiniband Spec for input signal conditions

Table 85 FDR limiting active cable output electrical specifications

Symbol	Parameter	Specification value(s)	Unit	Conditions
X	eye mask parameter, time	0.30	UI	Hit ratio=5E-5 with 100 Ohm load at TP7a (Note [a])
Y1, Y2	Diff. unsigned output voltage range 0 (required) range 1 (optional) range 2 (optional)	50, 225 100, 350 150, 450	mV	
	Crosstalk signal Vpk-pk, each aggressor	700	mV	At TP6a. Counter-propagating aggressors.[b]
	Crosstalk signal transition time, 20%-80%	24	ps	

Symbol	Parameter	Max	Min	Unit	Conditions
Vout	Single-ended output voltage	4.0	-0.3	V	Referred to Signal Ground; measured at TP7a
V_{CM}	AC common mode output voltage (RMS)	20		mV	at TP7a
	Termination mismatch	5		%	1 MHz; at TP7a
S_{DD22}	Differential output return loss	Eq. 1 on page 287		dB	At TP7a, 50 MHz to 15 GHz
S_{CC22}	Common mode output return loss	-2		dB	At TP7a, 200 MHz to 15 GH
S_{DC22}	Common mode to differential reflection	Eq. 2 on page 287		dB	At TP7a, 50 MHz to 15 GHz
t_r, t_f	Output transition time		17	ps	20-80%
J2	J2 Jitter	0.44		UI	At TP7a
J9	J9 jitter	0.69		UI	At TP7a

a. Output range is set for QSFP+ interfaces using page 03, addresses 238 & 239; see Section 8.5.
For CXP interfaces, output range is set using Rx Addresses 62-67; see Section 8.7.0.2.
b. Please refer to CIWG Method of Implementation (MOI) document Active Time Domain Testing for detailed specification of testing methodology and parameters.

Figure 20. InfiniBand Spec for output signal conditions

Revision History

Revision	Release Date	Rev Notes
1.0.00	11/26/2013	Initial Release
1.0.01	12/3/2013	Updated document title and footer section
1.0.02	1/23/2014	Correct part # for DSA8300 and MCB in Table 1. Set MCB-1 cable to range zero for ATD testing. Added DB9 Pin information in Appendix 1. General editing of connection diagrams, removing unnecessary connections during cal.

Disclaimer