InfiniBand HDR (200G) Method of Implementation

Active Time Domain (ATD) Testing
Anritsu MP1900A Signal Quality Analyzer
Keysight DCA-X Wideband Sampling Scope
Test Equipment Images

MP1900A Signal Quality Analyzer

Keysight DCA-X Wideband Sampling Scope
Target Test Platform (Block Diagram)

Calibrate test equipment to create the following environment for testing Active Optical Cables. Victim signal to be calibrated with jitter and channel loss stressors in the presence of co-propagating and counter-propagating aggressor signals.
## Anritsu MP1900A Configuration

<table>
<thead>
<tr>
<th>Slot</th>
<th>Part #</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>-</td>
<td>MP1900A</td>
<td>SIGNAL QUALITY ANALYZER-R</td>
</tr>
<tr>
<td>1, 2</td>
<td>MU1810008</td>
<td>12.5 GHz 4port Synthesizer.</td>
</tr>
<tr>
<td>3, 4</td>
<td>MU1815008</td>
<td>Jitter Modulation Source.</td>
</tr>
<tr>
<td>5</td>
<td>MU196040B</td>
<td>PAM4 ED</td>
</tr>
<tr>
<td></td>
<td>MU196040B-001</td>
<td>32G baud</td>
</tr>
<tr>
<td></td>
<td>MU196040B-011</td>
<td>Equalizer</td>
</tr>
<tr>
<td></td>
<td>MU196040B-021</td>
<td>29G baud Clock Recovery</td>
</tr>
<tr>
<td></td>
<td>MU196040B-041</td>
<td>SER Measurement</td>
</tr>
<tr>
<td></td>
<td>MU196040B-042</td>
<td>FEC Analysis</td>
</tr>
<tr>
<td>6</td>
<td>MU196020A</td>
<td>PAM4 PPG</td>
</tr>
<tr>
<td></td>
<td>MU196020A-001</td>
<td>32G baud</td>
</tr>
<tr>
<td></td>
<td>MU196020A-011</td>
<td>4Tap Emphasis</td>
</tr>
<tr>
<td></td>
<td>MU196020A-030</td>
<td>Data Delay</td>
</tr>
<tr>
<td></td>
<td>MU196020A-040</td>
<td>Adjustable ISI</td>
</tr>
<tr>
<td></td>
<td>J1758A</td>
<td>ISI Board K</td>
</tr>
<tr>
<td></td>
<td>MU196020A-042</td>
<td>FEC Pattern Generation</td>
</tr>
<tr>
<td>7</td>
<td>MU196020A</td>
<td>PAM4 PPG</td>
</tr>
<tr>
<td></td>
<td>MU196020A-001</td>
<td>32G baud</td>
</tr>
<tr>
<td></td>
<td>MU196020A-011</td>
<td>4Tap Emphasis</td>
</tr>
<tr>
<td></td>
<td>MU196020A-030</td>
<td>Data Delay</td>
</tr>
<tr>
<td></td>
<td>MU196020A-040</td>
<td>Adjustable ISI</td>
</tr>
<tr>
<td></td>
<td>MU196020A-042</td>
<td>FEC Pattern Generation</td>
</tr>
<tr>
<td>8</td>
<td>MU183020A</td>
<td>28G/32G bit/s PPG.</td>
</tr>
<tr>
<td></td>
<td>MU183020A-001</td>
<td>32G bit/s Extension.</td>
</tr>
<tr>
<td></td>
<td>MU183020A-023</td>
<td>2ch 3.5V Data Out.</td>
</tr>
<tr>
<td></td>
<td>MU183020A-031</td>
<td>2ch Data Delay.</td>
</tr>
</tbody>
</table>
Scope Setting Overview

Not detailed in this document, the DCA-X must be pre-configured as follows before any calibration measurements are made.

1. Perform mainframe / module / time-base calibration.
2. Attach proper V (1.85mm) skew matched cable assemblies to scope channels. S-parameter data to 70GHz minimum must exist for each cable. This data used to compensate measurement channel.
3. Perform DCA-X channel de-skew procedure using pre-attached V measurement cables. Must use external trigger for this step. Scope CR cannot be used. Use manual hardware de-skew to fine-tune if necessary.
4. Adjust scope BW to 33GHz 4-th order Bessel response.
5. Configure scope math function to de-embed cables from the channel 1 (A) and channel 2 (B) measurement paths (remove s-parameters function). Use scope math function to create a differential signal (C) from the resulting cable de-embedded signals.
6. Configure Emulated Loss Channel (A) and CTLE block (B) when measuring DUT output parameters through far-end emulated channel.
7. AC-Common-Mode Voltage measurement must also be configured using scope math function.
8. After performing above steps, determine scope attenuation factors by measuring the difference between power meter and scope measurement of 6.445GHz CW signal. These differences are entered as external attenuation in the External HW section. See MOI worksheet tab for additional information.
Scope Figures Referenced in Previous Slide

Item 3

Item 4

Item 5

(A)

(B)

(C) (CTLE not used for aggressors)

Item 6

(A)

(B)

Item 7

Item 8
Target Test Platform (Diagram Implementation)

Final test platform as shown.

Single MP1900A mainframe provides all victim & aggressor signals to test fixtures and Cable Under Test.

Error Detector measures BER at DUT Rx1 output
DCA measures quality of signal at DUT RX2 output.

DUT I2C interfaces controlled by Aardvarks.

Numbers are cross-referenced to Equipment List table.
<table>
<thead>
<tr>
<th>Item #</th>
<th>Description</th>
<th>Vendor</th>
<th>Part #</th>
<th>Qty</th>
<th>Function / Details</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Signal Quality Analyzer</td>
<td>Anritsu</td>
<td>MP1900A</td>
<td>1</td>
<td>Signal Source for traffic and jitter impairments</td>
</tr>
<tr>
<td>2</td>
<td>Sampling Scope Mainframe</td>
<td>Keysight</td>
<td>DCA-X 86100</td>
<td>1</td>
<td>Scope Mainframe</td>
</tr>
<tr>
<td>3</td>
<td>Sampling Scope Module</td>
<td>Keysight</td>
<td>N1060A</td>
<td>1</td>
<td>Sampling module for all time domain measurements.</td>
</tr>
<tr>
<td>4</td>
<td>V Male - K Female Adaptors</td>
<td>Anritsu</td>
<td>34VKF50</td>
<td>4</td>
<td>Conversion from PPG1, PPG2 V to J1741A K</td>
</tr>
<tr>
<td>5</td>
<td>V Female - K Male Adaptors</td>
<td>Anritsu</td>
<td>34VFK50A</td>
<td>2</td>
<td>Conversion from MCB K to J1790A V</td>
</tr>
<tr>
<td>6</td>
<td>ISI Channel</td>
<td>Anritsu</td>
<td>J1758A</td>
<td>1</td>
<td>Fixed ISI Channel</td>
</tr>
<tr>
<td>7</td>
<td>MCB</td>
<td>Wilder Technologies</td>
<td>QSFP28-TPA100G-MCB-R</td>
<td>2</td>
<td>Module Compliance Board for AOC testing.</td>
</tr>
<tr>
<td>8</td>
<td>HCB</td>
<td>Wilder Technologies</td>
<td>QSFP28-TAP100G-HCB-P</td>
<td>1</td>
<td>Host Compliance Board (module) used for ATD calibration.</td>
</tr>
<tr>
<td>9</td>
<td>ATD Test Platform</td>
<td>Anritsu</td>
<td>AER-1004</td>
<td>1</td>
<td>Test platform to support for equipment / MCB / DUT connections</td>
</tr>
<tr>
<td>10</td>
<td>Power Divider</td>
<td>Anritsu</td>
<td>K240A</td>
<td>4</td>
<td>PPG signal division for driving all AOC lanes. Embedded inside AER-1004</td>
</tr>
<tr>
<td>11</td>
<td>Power Splitter</td>
<td>Anritsu</td>
<td>K241A</td>
<td>8</td>
<td>PPG signal division for driving all AOC lanes. Embedded inside AER-1004</td>
</tr>
<tr>
<td>12</td>
<td>K Cables, 0.24m</td>
<td>CW Swift</td>
<td>EP7024R-6</td>
<td>21</td>
<td>Interconnect cables for driving AOC lanes. Embedded inside AER-1004</td>
</tr>
<tr>
<td>13</td>
<td>K Cables, 0.8m</td>
<td>Anritsu</td>
<td>J1551A</td>
<td>2</td>
<td>Interconnect cables for aggressor signals. Skew matched pairs.</td>
</tr>
<tr>
<td>14</td>
<td>K Cables, 0.8m</td>
<td>Anritsu</td>
<td>J1741A</td>
<td>6</td>
<td>Interconnect cables for victim input &amp; output signals. Length specific cables.</td>
</tr>
<tr>
<td>15</td>
<td>V Cables, 0.8m</td>
<td>Anritsu</td>
<td>J1790A</td>
<td>2</td>
<td>Scope measurement cables. Length specific cables.</td>
</tr>
<tr>
<td>16</td>
<td>SMA Cables, 0.3m</td>
<td>Anritsu</td>
<td>J1349A</td>
<td>4</td>
<td>Interconnect cables for MP1800A Clocking and Scope Triggering</td>
</tr>
<tr>
<td>17</td>
<td>3dB Passive Equalizer</td>
<td>Anritsu</td>
<td>J1621A</td>
<td>4</td>
<td>Equalization for aggressor signals</td>
</tr>
<tr>
<td>18</td>
<td>I2C/SPI Host Adapter</td>
<td>Aardvark</td>
<td>TP240141</td>
<td>2</td>
<td>AOC Programming</td>
</tr>
<tr>
<td>19</td>
<td>Clip Lead Set</td>
<td>Aardvark</td>
<td>TP240411</td>
<td>2</td>
<td>Interfaces between DB9 and MCB terminal block for programming</td>
</tr>
<tr>
<td>20</td>
<td>3.3V/10W Supply</td>
<td>Phihong</td>
<td>PSAA20R-033</td>
<td>2</td>
<td>AOC Power Supplies</td>
</tr>
<tr>
<td>21</td>
<td>50 Ohm Terminations</td>
<td></td>
<td></td>
<td>-</td>
<td>Terminate unused ports during test and calibration</td>
</tr>
<tr>
<td>22</td>
<td>Synthesizer</td>
<td>Anritsu</td>
<td>MG3692C</td>
<td>1</td>
<td>Signal source for scope calibration</td>
</tr>
<tr>
<td>23</td>
<td>Power Meter</td>
<td>Anritsu</td>
<td>ML2437A</td>
<td>1</td>
<td>Power Meter Control Unit</td>
</tr>
<tr>
<td>24</td>
<td>Power Sensor</td>
<td>Anritsu</td>
<td>MA2482D</td>
<td>1</td>
<td>Power Sensor, 10MHz - 18GHz</td>
</tr>
</tbody>
</table>
Target Test Platform (Photo Implementation)
Loss Channel

Final loss channel selection to be made upon completion of all s-parameter measurements.
Final Loss Channel includes Wilder Tech QSFP28 MCB + HCB + Anritsu J1758A channel + J1741A cables.
PPG ISI function will be used to fine-tune tune to 10dB Insertion Loss. (Setting of -1.73dB to compensate for excess physical loss)

From IBTA Specification

\[ \text{Insertion Loss}(f) \leq \begin{cases} 0.05 + 1.8/f + 0.2705f & 0.01 \leq f \leq 13.28 \\ -4.0096 + 1.07f & 13.28 < f \leq 26.5625 \end{cases} \text{(dB)} \]  

where
- \( f \) is the frequency in GHz
- \( \text{Insertion Loss}(f) \) is the 200GAUI-4 or 400GAUI-8 chip-to-module insertion loss

Actual Test Data

Figure 120E-4—Recommended 200GAUI-4 or 400GAUI-8 chip-to-module channel insertion loss

Loss Channel for IBTA EDR / HDR

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I2C Interface

Notes:
- Discrete connection shown above using banana and clip lead cable assemblies.
- Custom cable assembly typically used at Plugfests which directly connects I2C signals & power across Aardvark, ATD test fixture and MCB.
### HDR Calibration (DUT Input)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Unit</th>
<th>Tol. (+/-)</th>
<th>Min</th>
<th>Nominal</th>
<th>Max</th>
<th>Window Size</th>
<th>Source</th>
</tr>
</thead>
<tbody>
<tr>
<td>Forward Data Rate</td>
<td>Gbaud</td>
<td>0.01%</td>
<td>-</td>
<td>26.56250</td>
<td>-</td>
<td>v2r1_4.171005.pdf</td>
<td></td>
</tr>
<tr>
<td>Counter FEXT Aggressors Vp-p</td>
<td>mV</td>
<td>5%</td>
<td>428</td>
<td>450</td>
<td>473</td>
<td>45</td>
<td>Table 103 v2r1_5.200930.pdf</td>
</tr>
<tr>
<td>Counter FEXT Aggressors</td>
<td>ps</td>
<td>18%</td>
<td>13.94</td>
<td>17.00</td>
<td>20.06</td>
<td>6.12</td>
<td>Table 103 v2r1_5.200930.pdf</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>HDR DUT Parameter</th>
<th>Unit</th>
<th>Min</th>
<th>Max</th>
<th>Source</th>
</tr>
</thead>
<tbody>
<tr>
<td>Near-End Eye Symmetry Mask Width</td>
<td>UI p-p</td>
<td>0.265</td>
<td>-</td>
<td>Table 104 v2r1_5.200930.pdf</td>
</tr>
<tr>
<td>Far-End Eye Symmetry Mask Width</td>
<td>UI p-p</td>
<td>0.200</td>
<td>-</td>
<td>Table 104 v2r1_5.200930.pdf</td>
</tr>
</tbody>
</table>

### Forward Traffic Eye Height

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Unit</th>
<th>Min</th>
<th>Max</th>
<th>Window Size</th>
<th>Source</th>
</tr>
</thead>
<tbody>
<tr>
<td>Forward Traffic Eye Height</td>
<td>mV</td>
<td>5%</td>
<td>30</td>
<td>34</td>
<td>3 Table 103 v2r1_5.200930.pdf</td>
</tr>
<tr>
<td>Forward Traffic Eye Width</td>
<td>UI p-p</td>
<td>5%</td>
<td>0.209</td>
<td>0.231</td>
<td>0.022 Table 103 v2r1_5.200930.pdf</td>
</tr>
<tr>
<td>Far-End Eye Height</td>
<td>mV</td>
<td>5%</td>
<td>836</td>
<td>880</td>
<td>888 Table 104 v2r1_5.200930.pdf</td>
</tr>
</tbody>
</table>

### Compliance (DUT Output)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Unit</th>
<th>Min</th>
<th>Max</th>
<th>Source</th>
</tr>
</thead>
<tbody>
<tr>
<td>BER</td>
<td>-</td>
<td>-</td>
<td>1.00E-05</td>
<td>Error Free. Lane 0. Working Group Discussions</td>
</tr>
<tr>
<td>AC common mode output voltage</td>
<td>mV</td>
<td>-</td>
<td>20</td>
<td>Table 104 v2r1_5.200930.pdf</td>
</tr>
</tbody>
</table>
Calibration Step 1: Set Baseline PPG Jitter

Intrinsic jitter characteristics targets for Random Jitter, Bounded Uncorrelated Jitter (BUJ), Odd/Even Jitter and Sinusoidal Jitter (SJ) are adjusted and verified in this calibration step. Signal measured directly at the output of the pattern generator. Red elements indicate the relevant signal sources, paths and measurement equipment.

<table>
<thead>
<tr>
<th>Instruments to Adjust</th>
<th>Setting Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>MU196020A PPG1, Channel 1</td>
<td>MU196020A: Set amplitude, level balance, HPJ, QPRBS13 pattern</td>
</tr>
<tr>
<td>MU181500B Jitter Module</td>
<td>MU181500B BUJ: Bit Rate 2.65625 Gb/s, 200MHz, PRBS7 (for baseline J4u)</td>
</tr>
<tr>
<td></td>
<td>MU181500B SJ1: Frequency = 91MHz (50mUI per tolerance chart)</td>
</tr>
<tr>
<td></td>
<td>MU181500B SJ2: Frequency = 87MHz (for baseline Jrms)</td>
</tr>
<tr>
<td></td>
<td>MU181500B RJ: Unfiltered (baseline)</td>
</tr>
<tr>
<td>Objective: Determine jitter set points to achieve calibration targets as measured by DCA-X</td>
<td></td>
</tr>
</tbody>
</table>
| Sample measurements shown in scope images (RLM, Eye Width, DJ, J4u, Jrms, EOJ)
Calibration Step 2: Counter-Prop FEXT Aggressors

Set counter-propagating aggressor crosstalk for the victim calibration in later steps. Counter-propagating aggressor signals are applied into the HCB and measured at corresponding points on MCB-1 using the scope. Red elements indicate the relevant signal sources, paths and measurement equipment.

<table>
<thead>
<tr>
<th>Instruments to Adjust</th>
<th>Setting Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>MU183020A, PPG4, Channel 2</td>
<td>MU183020A: Calibrate using PRBS10. Final Test using PRBS31 pattern. Objective: Determine amplitude set point to achieve calibration targets as measured by DCA-X. Sample measurements shown in scope images (Histogram Peak-Peak, Rise Time, Fall Time).</td>
</tr>
</tbody>
</table>
Calibration Step 3: Co-Prop FEXT Aggressors

Set co-propagating aggressor crosstalk for the victim calibration in later steps. Co-propagating aggressor signals are applied into the MCB and measured at corresponding points on HCB using the scope. Red elements indicate the relevant signal sources, paths and measurement equipment.

<table>
<thead>
<tr>
<th>Instrument to Adjust</th>
<th>Setting Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>MU196020A, PPG1</td>
<td>MU18x020A: Calibrate using PRBS10. Final Test using PRBS31 pattern.</td>
</tr>
<tr>
<td>MU183020A, PPG2, Channel 1</td>
<td>Objective: Determine amplitude set point to achieve calibration targets as measured by DCA-X Sample measurements shown in scope images (Histogram Peak-Peak, Rise Time, Fall Time)</td>
</tr>
</tbody>
</table>
Calibration Step 4: Scope CTLE Setting

The DCA-X CTLE function simulates the DUT CTLE. Find DCA-X CTLE setting to produce maximum Eye Width x Eye Height product at specified BER. That CTLE Setting must be used for Final Victim Eye Width / Height Calibration.

Instrument to Adjust

No PPG set points adjusted here.
Apply ALL previous calibrated signals shown in red.

Setting Notes

Advance through all scope CTLE Settings to find the maximum Eye Width x Eye Height product. Select ONLY IEEE 802.3bs CDAUI-8 Presets in 0.5dB steps (when needed).

<table>
<thead>
<tr>
<th>CTLE</th>
<th>EW</th>
<th>EH</th>
<th>Product</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>1</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>2</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>3</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>4</td>
<td>70</td>
<td>6</td>
<td>420</td>
</tr>
<tr>
<td>5</td>
<td>184</td>
<td>33</td>
<td>6072</td>
</tr>
<tr>
<td>5.5</td>
<td>209</td>
<td>45.8</td>
<td>9572.2</td>
</tr>
<tr>
<td>6</td>
<td>227</td>
<td>58.7</td>
<td>12870.9</td>
</tr>
<tr>
<td>6.5</td>
<td>232</td>
<td>58.7</td>
<td>19618.4</td>
</tr>
<tr>
<td>7</td>
<td>218</td>
<td>53.3</td>
<td>12055.4</td>
</tr>
<tr>
<td>8</td>
<td>204</td>
<td>45</td>
<td>9180</td>
</tr>
<tr>
<td>9</td>
<td>176</td>
<td>30.8</td>
<td>5420.8</td>
</tr>
</tbody>
</table>

![Diagram of calibration setup with CTLE settings and readings]
Calibration Step 5: Final Eye Width/Height

Achieve eye width and height calibration targets with all stressors and aggressor traffic enabled. All measurements to be performed at previously determined scope CTLE setting.

<table>
<thead>
<tr>
<th>Instrument to Adjust</th>
<th>Setting Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>MU196020A PPG1, Channel 1</td>
<td>MU196020A: Set amplitude to achieve final Eye Height</td>
</tr>
<tr>
<td>MU181500B Jitter Module</td>
<td>MU181500B RJ: Set amplitude to achieve final Eye Width</td>
</tr>
<tr>
<td>Sample measurements shown in scope images (Eye Width, Eye Height)</td>
<td></td>
</tr>
</tbody>
</table>
Calibration Step 6: Counter-Prop NEXT Aggressors

Set counter-propagating aggressor crosstalk for the victim calibration in later steps.
Counter-propagating aggressor signals are applied into the HCB and measured at corresponding points on MCB-2 using the scope.
Red elements indicate the relevant signal sources, paths and measurement equipment.

<table>
<thead>
<tr>
<th>Instruments to Adjust</th>
<th>Setting Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>MU183020A, PPG4, Channel 2</td>
<td>MU183020A: Calibrate using PRBS10. Final Test using PRBS31 pattern. Objective: Determine amplitude set point to achieve calibration targets as measured by DCA-X Sample measurements shown in scope images (Histogram Peak-Peak, Rise Time, Fall Time)</td>
</tr>
</tbody>
</table>
Compliance Test

Test DUT as shown, applying all stressors and aggressor traffic as previously calibrated.

Final Test Notes:
1. Software Forge EEPROM Command Center (ECC) used to configure DUT for proper ranges, CTLE, and clock recovery settings.

2. Final DUT parameters include:
   - BER
   - Near & Far end Eye Width Mask Symmetry (Far-end is emulated in scope using channel model)
   - Near & Far end Eye Height (Far-end is emulated in scope using channel model)
   - Transition Speed per specification
   - AC Common-Mode Output Voltage
HDR Compliance Specifications

Scope auto-measurements to determine parameters:
- ESMEn, ESMEf
- EHn, EHf
- Far-end pre-cursor ISI ratio

MP1900A to determine parameters:
- Bit Error Rate
- PAM4 Symbol Error Rate
- FEC Symbol Error Rate
- FEC Uncorrectable Error Rate

### Table 104 HDR limiting active cable output electrical specifications

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Specification value(s)</th>
<th>Unit</th>
<th>Conditions/Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Crosstalk signal V pk-pk, each aggressor</td>
<td>860 +/- 10%</td>
<td>mV</td>
<td>At TP5a. Counter-propagating aggressors. Transition time measured at PRBS13Q positions given in 802.3 120E 3.1.5</td>
</tr>
<tr>
<td></td>
<td>Crosstalk signal transition time, 20%-80%</td>
<td>17 +/- 3</td>
<td>ps</td>
<td></td>
</tr>
</tbody>
</table>

Table 6.9.2.4.2 HDR LIMITING ACTIVE CABLE OUTPUT REQUIREMENTS

Each electrical output lane and signal of the HDR active cable when measured at TP7a shall meet the specifications of Table 104 while the signals on all input lanes at the other end of the cable comply with the specifications of Table 103 on page 386 and the specified crosstalk signals are applied to all lanes of the active cable's electrical input at the output end of the cable. The active cable electrical output shall be AC coupled; i.e. it shall present a high DC common-mode impedance at TP7a. There may be various methods for AC coupling in actual implementations.

![Figure 96 Module compliance board test points, pluggable module](image)

- Please refer to CIWS Method of Implementation (MOI) document Active Time Domain Testing for detailed specification of testing methodology and parameters.